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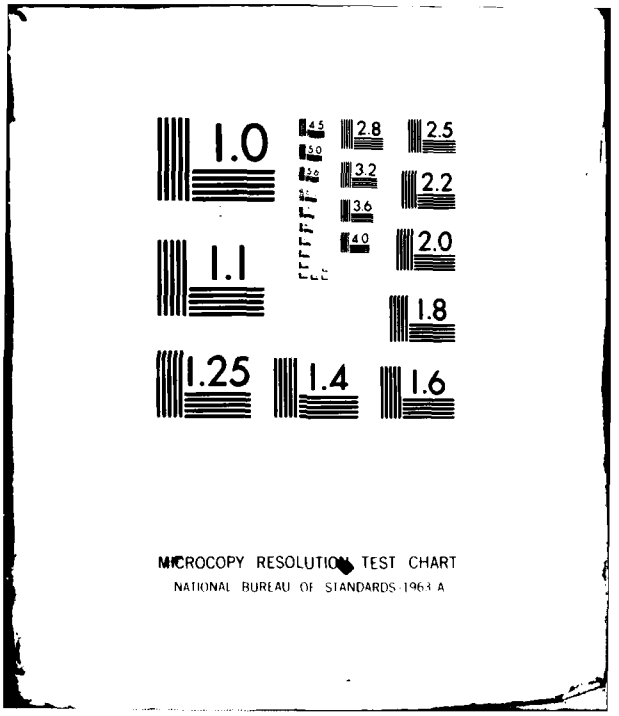
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1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A085 753
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) (6) STUDY OF A COMPUTER ASSISTED TEST PROGRAM	5. TYPE OF REPORT & PERIOD COVERED (9) Technical Report
	6. PERFORMING ORG. REPORT NUMBER (14) R-869; UILU-ENG-78-2263
7. AUTHOR(s) (10) Adel A. Sakla	8. CONTRACT OR GRANT NUMBER(s) (15) N68335-78-C-0524; N00014-79-C-0424
9. PERFORMING ORGANIZATION NAME AND ADDRESS Coordinated Science Laboratory University of Illinois at Urbana-Champaign Urbana, Illinois 61801	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS (12) 136
11. CONTROLLING OFFICE NAME AND ADDRESS Joint Services Electronics Program	12. REPORT DATE (11) Dec[illegible]79
	13. NUMBER OF PAGES 141
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report)
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Fault Analysis
Analog Circuits

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

As systems become more and more complex, the need for good fault diagnostic procedures becomes more obvious. In recent years much work has been done on the fault analysis of digital circuits, primarily because the growth in the size of these circuits has necessitated good fault diagnostic tests. The two state nature ("1" or "0") of digital circuits has also made them more amenable to the development of reasonably simple and reliable test procedures. In contrast, research on fault diagnostic procedures for analog circuits has not been as fruitful, nor have the pressures to develop good fault diagnostic tests for

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20. ABSTRACT (continued)

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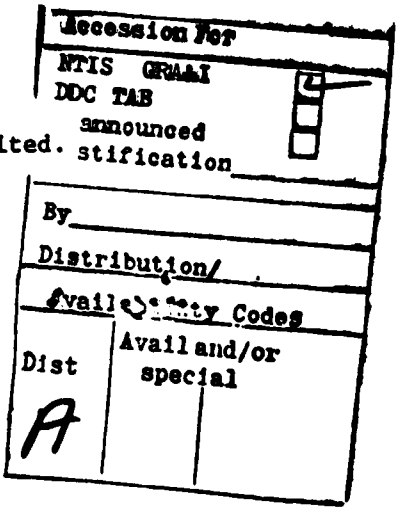
UILU-ENG 78-2263

STUDY OF A COMPUTER ASSISTED TEST PROGRAM

by

Adel A. Skala

This work was supported in part by the U.S. Naval Air Engineering Center under Contract N68335-78-C-0524 and in part by the Joint Services Electronics Program (U.S. Army, U.S. Navy and U.S. Air Force) under Contract N00014-79-C-0424.



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CHAPTER 1

INTRODUCTION

As systems become more and more complex, the need for good fault diagnostic procedures becomes more obvious. In recent years much work has been done on the fault analysis of digital circuits, primarily because the growth in the size of these circuits has necessitated good fault diagnostic tests. The two state nature("1" or "0") of digital circuits has also made them more amenable to the development of reasonably simple and reliable test procedures. In contrast, research on fault diagnostic procedures for analog circuits has not been as fruitful, nor have the pressures to develop good fault diagnostic tests for analog circuits been as great due to their relatively small number of components in comparison with digital systems.

Presently there is a great interest in the automatic testing and fault analysis of electrical circuits because of the availability of low-cost computer systems. This report addresses itself only to the analog circuit testing problem.

It has been difficult to obtain a solution to the fault analysis problem because (a) usually the restriction is imposed that connections cannot be broken which means that currents cannot be measured reliably , and (b) the responses in a circuit are nonlinearly related to the parameter values of the circuit. Due to these difficulties the practical approach to fault analysis has been to generate fault

dictionaries. In this approach the circuit is simulated with a number of different fault conditions and the responses are compiled in a dictionary. The problem with this approach is that it requires excessive computation time and massive storage. For example, if a circuit has p parameters, and if one assumes n different possible values for each parameter, then $(n)^p$ simulations would be required to generate the dictionary. In order to avoid excessive computation time and massive storage, it is usually necessary to consider only a small number of possible faults so that the number of computer simulations required is not excessive.

In the second chapter, we review some of the previous work in the fault analysis of analog circuits. We review briefly different approaches together with their advantages and disadvantages.

A new approach for the fault analysis of linear analog circuits based on the adjoint circuit concept will be presented in detail in the third chapter. The approach requires the measurement of all node voltages under certain test conditions. In addition, the simulation of the adjoint circuit on the computer is required. The approach has the advantage of detecting possibly large tolerances. It is also highly computationally efficient, and it does not require massive storage. Moreover, the formulation allows one to determine necessary and sufficient test conditions to determine the component values.

In the fourth chapter, we adapt the same approach to deal with fault detection in analog circuits with accessibility to only part of the nodes. A major application, single fault identification, will be discussed in detail. It is shown that input and output voltage measurements are enough to identify single faults.

The extension of the approach to the fault analysis of analog circuits with some nonlinear elements is discussed in the fifth chapter. It is shown that we can determine any number of operating points on the I-V characteristic of the faulty nonlinear elements.

Some numerical examples are presented to demonstrate the different algorithms in the sixth chapter. The conclusion follows in the seventh chapter.

CHAPTER 2

PREVIOUS WORK IN THE FAULT ANALYSIS OF ANALOG CIRCUITS

2.1 INTRODUCTION

The problem of fault analysis of analog circuits has been attacked for many years from different sides. The fault analysis problem requires the determination of circuit parameter values from some measurements. Many different approaches and theorems have been presented in the literature. In this chapter we will review some of the approaches for the fault analysis of analog circuits together with some theorems for solvability. They will be categorized into two main categories. The first category is when all the circuit nodes are accessible. By an accessible node we mean a node whose voltage can be measured, and any type of excitation (voltage or current source) can be applied to the circuit at that node with respect to a reference node. The second category is when we have only a subgroup of the nodes that are accessible, while the rest of nodes are not. The advantages and disadvantages of each method will be discussed.

2.2 PREVIOUS WORK AND THEOREMS FOR SOLVABILITY

2.2.1 ACCESSIBILITY TO ALL CIRCUIT NODES

In this section we will review some of the previous work done for

fault analysis assuming that all the circuit nodes are accessible.

2.2.1.1 METHODS FOR ELEMENT ISOLATION

The determination of the value of an element is not difficult if both the current through the element and the voltage across the element can be measured. In order to determine the current through an element, one terminal of the element must be isolated. This can be done by breaking the connection at one end of the element, but this approach is not considered practical in most test situations. However, in this section, three other methods [1] are given for effectively isolating an element which do not require that conductive paths be broken.

Consider the circuit in Figure 2.1. The unknown element is connected between the nodes numbered 1 and 2. The impedances Z_a through Z_m lie on paths which ultimately return to node 1. Let us inject a current I into node 2. The element Z_0 can be isolated by shorting nodes 3 to k, connecting a voltage source to node 3, and adjusting the value of the voltage source until $V_2=V_3$ as shown in Figure 2.2. Then,

$$Z_0 = V_{21}/I \qquad \ldots.(2.1)$$

The disadvantage of this approach is that it requires the shorting of nodes in the circuit, and furthermore, the voltage source must be adjusted iteratively until $V_2=V_3$.

A second approach which does not require an iterative adjustment consists of shorting nodes 3 to k, and applying a voltage source between nodes 3 and 1, as shown in Figure 2.3. For this circuit,

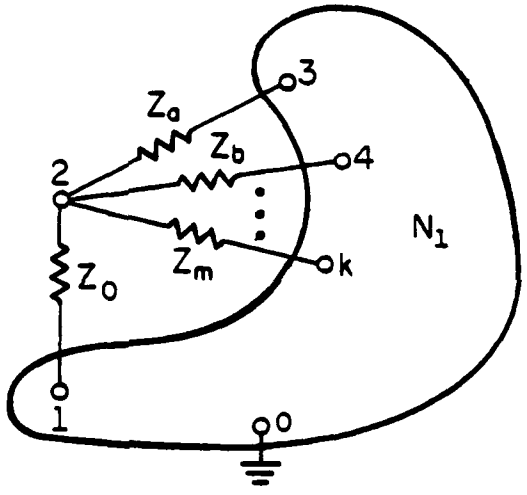


Fig. 2.1 Arbitrary network containing Z_o.

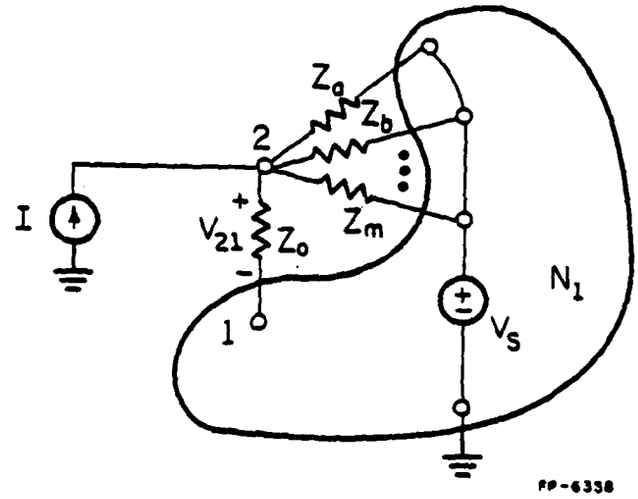


Fig. 2.2 Equipotential method for element isolation.

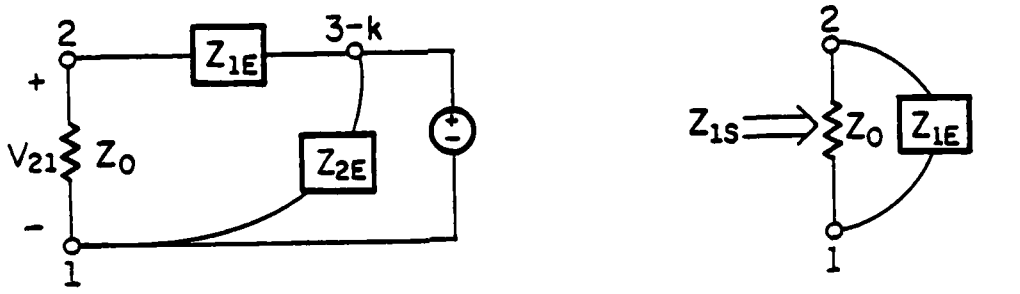


Fig. 2.3 Determination of Z_o without iterative adjustments of the voltage source.

$$(V_{21}/V_s) = Z_0/(Z_{1E}+Z_0) \qquad ....(2.2)$$

Note that Z_{1E} is the equivalent impedance of the parallel combination of impedances Z_a through Z_m. Next, nodes 3 through k are shorted to node 1 as shown in Figure 2.3, and the impedance

$$Z_{1s} = (Z_{1E}\ Z_0)/(Z_{1E}+Z_0) \qquad ....(2.3)$$

is measured. From Eqs. (2.2) and (2.3) we obtain

$$Z_0 = Z_{1s}/(1-(V_{21}/V_s)) \qquad ....(2.4)$$

Thus, the unknown impedance Z_0 can be determined from a two-step measurement procedure. The accuracy of the method deteriorates when the voltage ratio V_{21}/V_s is nearly unity, or equivalently , $|Z_{1E}| << |Z_0|$.

Finally, a third approach to isolating an element consists of connecting the element Z_0 to the negative input terminal of a high gain amplifier and grounding nodes 3 through k, as shown in Figure 2.4. Ideally, the amplifier would have infinite gain and zero offset so that node 2 is a virtual ground. Thus, assuming negligible current through the impedances $Z_a, Z_b, \ldots\ldots, Z_m$ we obtain

$$Z_0 = -R_{ref}\ V_s/\ V_0 \qquad ....(2.5)$$

This method requires only one measurement. The Hewlett-Packard 3060A Board Test System uses a sophisticated version of this node isolation technique to make in-circuit component measurement.

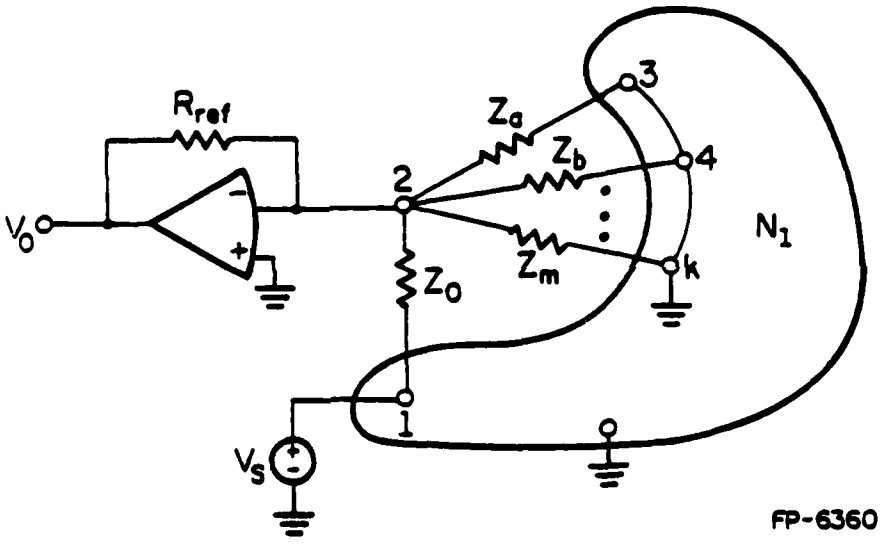


Fig. 2.4 Isolation with a high gain amplifier.

2.2.1.2 LARGE CHANGE SENSITIVITY RELATIONSHIP

Attacking the problem in a reverse manner, R. N. Gadenz, M. G. Rezai-Fakhr, and G. C. Temes [2], 1973, used a relation between the voltage and current changes in the original circuit due to possibly large parameter changes, and the voltages and currents of the adjoint circuit in order to compute voltage and current changes due to tolerance effects. They set up a reduced system of equations solvable by either Gaussian elimination or iteration to compute the response changes for specified element changes, regardless of whether or not they are small or large changes. They found out that their method was more economical and efficient in computation than the direct analysis method or any other method, provided that the number of toleranced parameters is much smaller than the number of equations needed for the direct analysis of the network.

2.2.1.3 SINGLE FAULT DETECTION IN POSITIVE RESISTOR CIRCUITS

An approach for single fault detection in positive resistor circuits was suggested by T. N. Trick and R. T. Chien [3]. In which, it was proved that for positive resistor circuits, if one and only one resistor changes from its nominal value, then the voltage across that resistor is greater than or equal to all the other resistor voltage changes.

2.2.1.4 A THEOREM ON SOLVABILITY

Studying the same problem from the graph theory point of view, W. Mayeda proved an important theorem [4] concerning impedance isolation. He stated that :"the measurement of the impedance Z_0 at its

terminals c and r is possible if and only if all paths in the circuit from node c to node r (excluding the path through Z_0) contain at least one accessible node." He proved this theorem using topological concepts; a slightly different proof was also discussed in [1].

2.2.1.5 THE ADJOINT CIRCUIT APPROACH

In this thesis, we present an additional approach to the calculation of element values when all the nodes in the circuit are accessible. This method is discussed in detail in the next chapter.

2.2.2 ACCESSIBILITY TO PART OF THE CIRCUIT NODES

In this section, we will review some of the previous work done for fault analysis assuming that not all of the circuit nodes are accessible. There are two main directions in this case; the first is concerned with pre-test procedures, while the second is concerned with post-test procedures.

2.2.2.1 PRE-TEST APPROACH

The pre-test approach is well-known as the fault dictionary method and is the most popular approach used in industry. In this approach faulty circuits with different fault combinations are simulated on the computer. Then, the different responses are compiled and a set of fault signatures are generated and stored. The correlation of actual test results with the stored data is used, hopefully, to identify the faulty elements. Different methods were proposed to implement this fault dictionary approach.

In 1966, S. Seshu and R. Waxman [5] gave a procedure for generating

a set of tests for conventional linear systems by means of gain measurements from an input terminal to an output terminal. Basically, the procedure was to compute the corner frequencies of the nominal network and choose, as test frequencies, several frequencies in the neighborhood of each corner frequency, and hence, detect shifts in the corner frequencies. Interpretation of measured values are obtained by precomputing the gain at these frequencies for parameter deviations from their nominal values, and compiling a fault dictionary. Two major disadvantages are, first, it needs the computation of the symbolic transfer function, and second, the computation time grows exponentially with the increase in circuit elements.

G. O. Martens, in 1972, developed a way for the identification of a single fault in electronic circuits [6]. They made use of the fact that, in a linear circuit, any transfer function can be expressed in terms of just one circuit parameter in a bilinear form. Graphical constructions of the transfer function loci are pre-plotted under different parameter changes, either experimentally or by circuit analysis using a digital computer. Then, simple magnitude and phase measurements, at a number of test frequencies, are made and plotted on the set of predetermined loci in the complex transfer-function plane. The faulty component and its parameter value may, then, be determined from the loci. The method is restricted to only single fault detection. It has some disadvantages; first, it requires considerable computational and graphical effort in order to plot the transfer function loci, especially when the circuit contains a high number of components. Second, it fails to detect faults in some elements at some frequencies. Third, it cannot point out single faults in a group of

different type elements connected in parallel. Finally, it does not have the capability of detecting relatively large single faults when the rest of the circuit parameters are within some prescribed tolerance.

A practical fault dictionary approach was given by R. E. Tucker and L. P. McNamee [7]. They developed fault models for some active devices, e.g. a transistor, where the faults occuring were catastrophic , i.e. either an open or short circuit. Then, they used these models in running computer aided analysis programs for the probable fault conditions. Next, they divided the different faults into groups, where each group was characterized by some certain faulty responses. Hence, using this information and the data obtained from the test circuit, they could detect and isolate catastrophic faults. Their method is basically the fault dictionary approach, which requires one to consider only a limited number of possible faults in order to avoid excessive computation. The method is a brute force approach which only yields information about the number and placement of test points through numerous computer simulation.

Another similar approach is given in [8].

2.2.2.2 POST-TEST APPROACH

The post-test approach does not require any pre-test data. It is performed after the test measurements have been made and consists of solving a set of nonlinear equations.

In 1962, R. S. Berkowitz [9] initiated one of the first theoretical studies of the analog circuit fault analysis problem. He mathematically defined the concept of network-element-value solvability. Specifically, he established a set of definitions which enabled an objective

discussion of network solvability of arbitrary passive, linear, lumped parameter networks with respect to a restricted set of external terminals (available and partly available). Then, he obtained a relation between the number of available and partly available terminals of a network, and the number of admittance functions determining the measurable behavior of the network. Moreover, he introduced some theorems that gave solvability conditions for purely resistive networks with extension to include networks with internal energy sources. Finally, he obtained a general necessary condition for network-element-value solvability. Unfortunately, his work, 1) only gave some necessary conditions for network solvability, 2) lacked algorithms for network element evaluation, and 3) did not include active elements.

S. W. Director and R. A. Rohrer [10], 1969, attacked the problem from the design point of view. They introduced an automated network design algorithm in the frequency domain. In that algorithm, they started with an initial guess to the network structure and associated element values. Next, they considered a weighted integral square error criterion over a specified frequency range as a performance measure. By means of Tellegen's theorem [11,12], they derived a relation between the voltage and current changes in the circuit due to parameter changes and the voltages and currents of the adjoint circuit [13]. Then, they calculated the parameter space error gradient using that relation along with only two analyses for both the original and the adjoint circuits over that specified frequency range. Next, they adjusted the element values, i.e. tuned them, using a suitable optimization technique such that they moved in the negative gradient direction. Finally, they

repeated this process until a suitable termination criterion was met. This algorithm had two disadvantages; first, it took much computer time, and second, since only first-order sensitivity information is utilized, the algorithm can have serious convergence problems.

A fault isolation scheme via component simulation was proposed by R. Saeks [14], in 1972. By assuming an appropriate algebraic connection model matrix, a system could be separated into two different blocks, components and connections blocks. A formulation of the system's variables is constructed based on that separation. Then another system is designed to augment the original system, such that the whole augmented system behaves exactly the same as the components of the original system. Hence, by controlling the inputs to that augmented system and observing its outputs, component parameters could be determined. Using this formulation, they obtained the algebraic necessary and sufficient conditions for the exact determination of the internal component parameters for both the single-test frequency and multiple-test frequency cases. The main disadvantages of such a scheme are that, it requires an extremely large number of measurements. It also requires considerable computational effort for inverting some matrices, whose sizes are proportional to the dimension of the system. Moreover, it is not very practical for the given test conditions, since it requires the measurement of both branch currents and branch voltages.

Other approaches are discussed in [15].

CHAPTER 3

THE ADJOINT CIRCUIT APPROACH

3.1 INTRODUCTION

In this chapter, a new algorithm is proposed for the calculation of the element values in a linear circuit from node voltage measurements. The method requires the measurement of the node voltages of the circuit under several different test conditions. In addition, the simulation of a second circuit, the adjoint circuit, is required under various short-circuit constraints. The adjoint circuit simulations need to be made only once for any given circuit, and the results can be stored for future use. The element values of the test circuit can be easily computed from the node voltage measurements on the test circuit and the responses obtained from the adjoint circuit simulations.

3.2 THE ADJOINT CIRCUIT APPROACH

To derive the algorithm, consider the linear circuit N in Figure 3.1, which has m ports available. One may connect voltage or current sources to these ports or simply make open-circuit voltage measurements at these ports. We will assume that it is not practical to make short-circuit current measurements, because if this is the case , then by placing such a port in series with each element, the branch currents are measurable and the problem becomes trivial. In addition, short-circuiting some nodes while doing measurements may cause some

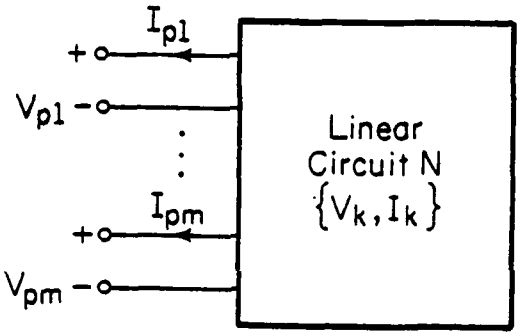


Fig. 3.1 Linear circuit with m input,output,or test ports.

damages to the circuit, e.g. burning some junctions due to excessive currents. Also, we assume that the circuit N has b internal branches whose respective branch voltages and currents in the frequency domain are denoted by $\{V_k, I_k\}$. Finally, we introduce a second circuit $\hat{N}$ [11,12,16], shown in Figure 3.2, which has the same topology as N, but not necessarily the same branch or port constraints. It is assumed that these circuits obey Kirchhoff's laws so that by means of Tellegen's conservation of power theorem we can write [11,12,26]

$$\sum_{k=1}^{b} (\hat{V}_k I_k - V_k \hat{I}_k) = - \sum_{j=1}^{m} (\hat{V}_{pj} I_{pj} - V_{pj} \hat{I}_{pj}) \qquad ....(3.1)$$

Now suppose that one or more faults occur in the circuit N so that $V_k \longrightarrow V_k + \Delta V_k$, $I_k \longrightarrow I_k + \Delta I_k$, $V_{pj} \longrightarrow V_{pj} + \Delta V_{pj}$,and $I_{pj} \longrightarrow I_{pj} + \Delta I_{pj}$. Eq. (3.1) becomes

$$\sum_{k=1}^{b} [\hat{V}_k (I_k + \Delta I_k) - (V_k + \Delta V_k) \hat{I}_k] =$$

$$- \sum_{j=1}^{m} [\hat{V}_{pj} (I_{pj} + \Delta I_{pj}) - (V_{pj} + \Delta V_{pj}) \hat{I}_{pj}] \qquad ....(3.2)$$

Subtracting Eq. (3.1) from Eq. (3.2), we obtain

$$\sum_{k=1}^{b} (\hat{V}_k \Delta I_k - \Delta V_k \hat{I}_k) = - \sum_{j=1}^{m} (\hat{V}_{pj} \Delta I_{pj} - \Delta V_{pj} \hat{I}_{pj}) \qquad ....(3.3)$$

Thus, by means of Tellegen's theorem, one can obtain a relationship between the voltage and current changes in the original circuit, due to

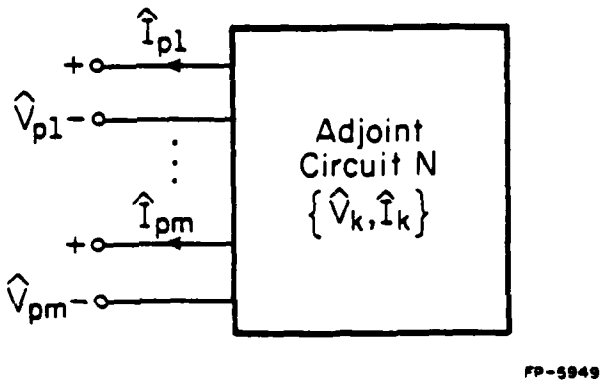


Fig. 3.2 Adjoint circuit of the circuit under test.

parameter changes in that circuit, and the voltages and currents of the adjoint circuit [1,17,18,19]. Eq. (3.3) is valid for both frequency and time domain measurements.

Next, we need to introduce the branch constraints into Eq. (3.3). Since we have assumed that only voltage measurements are available, we will assume that we can express every branch current as a function of its branch voltage.

If we assume that the kth branch corresponds to an admittance whose nominal value is Y_k, then we will have

$$I_k = Y_k V_k \qquad \ldots.(3.4)$$

and with faults

$$I_k + \Delta I_k = (Y_k + \Delta Y_k)(V_k + \Delta V_k) \qquad \ldots.(3.5)$$

Therefore

$$\Delta I_k = \Delta Y_k(V_k + \Delta V_k) + Y_k \Delta V_k \qquad \ldots.(3.6)$$

where V_k denotes the kth branch voltage when the circuit has no faulty component, i.e. with nominal values. Furthermore, let us choose the kth branch constraint of the circuit $\hat{N}$ such that it is the adjoint circuit of N [11,12,16], that is

$$\hat{I}_k = Y_k \hat{V}_k \qquad \ldots.(3.7)$$

Then we obtain

$$\hat{V}_k \Delta I_k - \Delta V_k \hat{I}_k = (V_k + \Delta V_k)\hat{V}_k \Delta Y_k \qquad \ldots.(3.8)$$

In Eq. (3.8) we assume that we can measure the branch voltage $V_k + \Delta V_k$, and the admittance change ΔY_k is the unknown.

Similarly, if we assume that the kth branch corresponds to a voltage controlled voltage source (VCVS), whose nominal value is μ_k, we will have

$$I_{\alpha k} = 0 \quad \text{,and} \quad V_{\beta k} = \mu_k V_{\alpha k} \qquad \ldots.(3.9)$$

and with faults

$$I_{\alpha k} + \Delta I_{\alpha k} = 0 \quad \text{,and} \quad V_{\beta k} + \Delta V_{\beta k} = (\mu_k + \Delta\mu_k)(V_{\alpha k} + \Delta V_{\alpha k}) \qquad \ldots(3.10)$$

Therefore,

$$\Delta I_{\alpha k} = 0 \quad \text{,and} \quad \Delta V_{\beta k} = \Delta\mu_k (V_{\alpha k} + \Delta V_{\alpha k}) + \mu_k \Delta V_{\alpha k} \qquad \ldots(3.11)$$

where α refers to the controlling branch and β refers to the controlled branch. Moreover, let us choose the kth branch constraint of the circuit $\hat{N}$ such that it is the adjoint circuit of N, that is a current controlled current source (CCCS) with

$$\hat{I}_{\alpha k} = -\mu_k \hat{I}_{\beta k} \quad \text{,and} \quad \hat{V}_{\beta k} = 0 \qquad \ldots(3.12)$$

Then, we obtain

$$\hat{V}_{\alpha k}\,\Delta I_{\alpha k} - \Delta V_{\alpha k}\hat{I}_{\alpha k} + \hat{V}_{\beta k}\,\Delta I_{\beta k} - \Delta V_{\beta k}\hat{I}_{\beta k}$$

$$= -\,(V_{\alpha k} + \Delta V_{\alpha k})\hat{I}_{\beta k}\,\Delta\mu_k \qquad \ldots(3.13)$$

where in Eq.(13) we assume we can measure the controlling branch voltage $V_{\alpha k} + \Delta V_{\alpha k}$, and the coefficient change $\Delta\mu_k$ is the unknown.

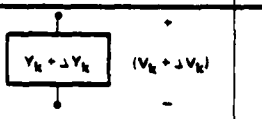
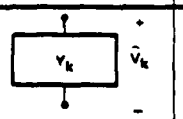
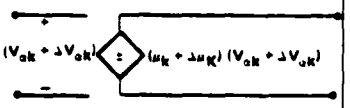
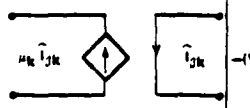
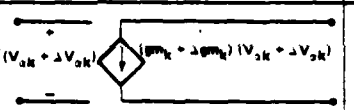
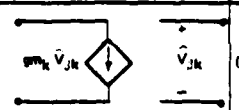
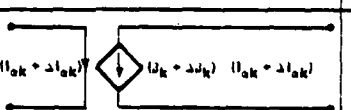
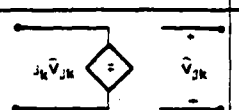
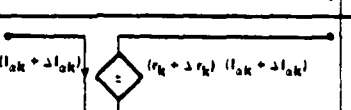
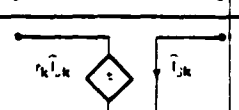
Similar expressions can be easily obtained for other controlled sources; voltage controlled current source (VCCS), current controlled current source (CCCS), and current controlled voltage source (CCVS). They are given in Table I.

Hence, Eq. (3.3) will reduce to

$$\sum_{k=1}^{b} (X_k + \Delta X_k)\hat{X}_k\,\Delta P_k = -\sum_{j=1}^{m} (\hat{V}_{pj}\,\Delta I_{pj} - \Delta V_{pj}\hat{I}_{pj}) \qquad \ldots(3.14)$$

where $X_k + \Delta X_k$ is assumed to be measured, $\hat{X}_k$ is assumed to be calculated from the adjoint circuit analysis, and ΔP_k is the unknown parameter change. These quantities are defined in Table I for different circuit elements. Eq. (3.14) is a linear equation in the unknown ΔP_k, $k=1,2,\ldots,b$. In order to solve for the ΔP_k's we need to generate a set of simultaneous linear algebraic equations with a rank equal to the number of unknowns. This can be done by an appropriate choice of test conditions for the circuit N and its adjoint $\hat{N}$. This set of simultaneous independent linear algebraic equations will have the following form

TABLE I THE CIRCUIT CONSTRAINTS AND THE CONTRIBUTION TO THE RIGHT SIDE OF EQ. (3.14) FOR THE DIFFERENT CIRCUIT ELEMENTS.

Element	P_k	X_k	$\hat{X}_k$	Circuit Constraints		Contribution to Left side of Equation (3.14)
				Test Circuit	Adjoint Circuit	
Admittance G,C, Γ	Y_k	V_k	$\hat{V}_k$			$(V_k + \Delta V_k)\,\hat{V}_k\,\Delta Y_k$
VCVS	μ_k	V_{ak}	$-\hat{I}_{jk}$			$-(V_{ak} + \Delta V_{ak})\,\hat{I}_{jk}\,\Delta\mu_k$
VCCS	gm_k	V_{ak}	$\hat{V}_{jk}$			$(V_{ak} + \Delta V_{ak})\,\hat{V}_{jk}\,\Delta gm_k$
CCCS	β_k	I_{ak}	$\hat{V}_{jk}$			$(I_{ak} + \Delta I_{ak})\,\hat{V}_{jk}\,\Delta\beta_k$
CCVS	rk	I_{ak}	$-\hat{I}_{jk}$			$-(I_{ak} + \Delta I_{ak})\,\hat{I}_{jk}\,\Delta r_k$

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$$\left[\begin{array}{ccc|ccc} (X_1+\Delta X_1)\hat{X}_1 & \cdots & (X_n+\Delta X_n)\hat{X}_n & \cdots & (X_b+\Delta X_b)\hat{X}_b \\ \vdots & & \vdots & & \vdots \\ (x_1+\Delta X_1)\hat{X}_1 & \cdots & (X_n+\Delta X_n)\hat{X}_n & \cdots & (X_b+\Delta X_b)\hat{X}_b \\ \vdots & & \vdots & & \vdots \\ (X_1+\Delta X_1)\hat{X}_1 & \cdots & (X_n+\Delta X_n)\hat{X}_n & \cdots & (X_b+\Delta X_b)\hat{X}_b \end{array}\right]\left[\begin{array}{c}\Delta P_1 \\ \vdots \\ \Delta P_n \\ \vdots \\ \Delta P_b\end{array}\right]=\left[\begin{array}{c}\Delta e_1 \\ \vdots \\ \Delta e_n \\ \vdots \\ \Delta e_b\end{array}\right] \qquad \ldots(3.15)$$

where Δe_i represents the right-hand side of Eq. (3.14), and each equation has a different combination of test conditions for the circuit N, and its adjoint $\hat{N}$. In general, the matrix of the linear system (3.15) is full. Then, the computation effort to solve this system will increase rapidly as the dimension of the circuit increases. Hence, it will be a good idea if this system could be broken into smaller subsystems, as shown by the dashed line in Eq. (3.15). Since, the entries of such matrix are $(X_k+\Delta X_k)\hat{X}_k$, and since $(X_k+\Delta X_k)$ is a response to be measured, then, the only term we can have control on will be $\hat{X}_k$. This could be done by appropriate choice of the adjoint circuit excitation conditions in order to force some of these $\hat{X}_k$'s to be zero, e.g., if we choose the adjoint circuits such that $\hat{X}_{n+1}=\hat{X}_{n+2}=\ldots\ldots=\hat{X}_b=0$ in the first n-equations in system (3.15), then, we can solve the resulting nxn subsystem for the unknowns $\Delta P_1,\ldots\ldots,\Delta P_n$. By doing so, we can partition our bxb matrix into comparatively smaller submatrices. Consequently, the computational effort will be improved greatly by solving these small subsystems.

In other words, a special choice of the adjoint circuits $\hat{N}$ will isolate a group of elements. This group of elements consists of all elements in a cutset, for example, all the elements connected to a common node. In order to see how this is done, consider the circuit shown in Figure 3.3, where Y_1 through Y_n are connected to node 1. Here we will assume, for simplicity, that this group of elements are linear and passive. Although, active elements could be handled by the appropriate models and Table I. Suppose we wish to measure the deviation of all n of these admittances from their nominal values. In Figure 3.3, we will assume that node n+1 is the reference node, and we have introduced n test ports at which measurements can be made and excitations applied to the circuit. In order to isolate the admittances Y_1 through Y_n and simplify the calculations, the ports 2 through n are shorted and a 1A source is applied at port 1 in the adjoint circuit as shown in Figure 3.4. With these constraints, Eq. (3.14) becomes

$$\hat{V}_{p1} \sum_{k=1}^{b} (V_k + \Delta V_k)\ \Delta Y_k = \Delta V_{p1} \cdot 1A + \sum_{k=2}^{n} \Delta V_{pk} \hat{I}_{pk} \qquad \ldots(3.16)$$

or we can divide by $\hat{V}_{p1}$ and eliminate the adjoint circuit responses.

$$\sum_{k=1}^{n} (V_k + \Delta V_k)\ \Delta Y_k = -(Y_{10} + Y_{20} + \ldots + Y_{n0})\ \Delta V_{p1} + \sum_{k=1}^{n-1} Y_{k0}\ \Delta V_{p(k+1)} \qquad \ldots(3.17)$$

or

$$\sum_{k=1}^{n} (V_k + \Delta V_k)\ \Delta Y_k = -\sum_{k=1}^{n} Y_{k0}\ \Delta V_k \qquad \ldots(3.18)$$

Recall that V_k is the branch voltage in the circuit without faults. Y_{k0}

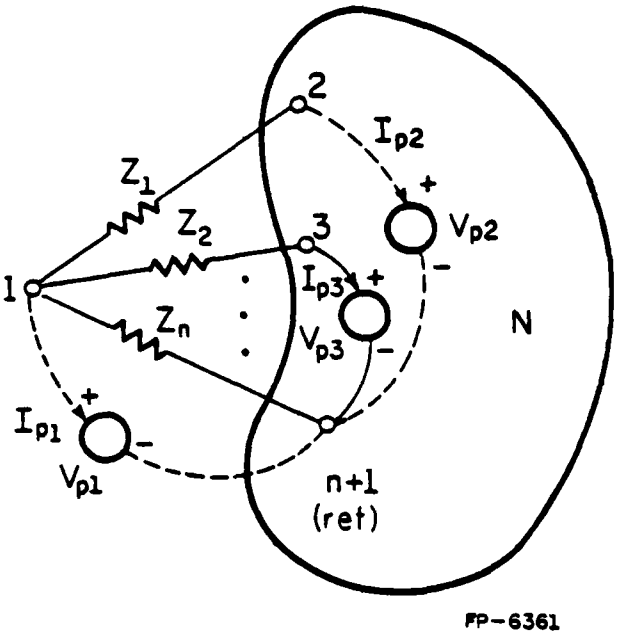


Fig. 3.3 Network with n unknown admittances connected to a common node.

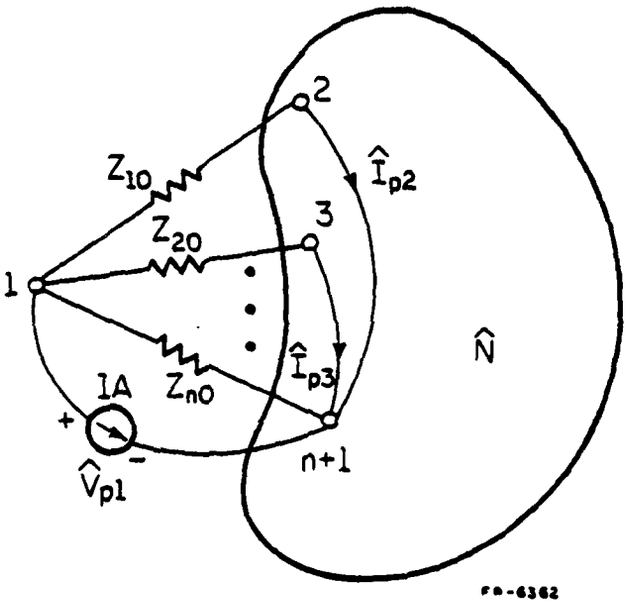


Fig. 3.4 Selection of the adjoint circuit port constraints to isolate the components Y_1 through Y_n.

is the nominal value of the admittance, and ΔV_k is the change in the branch voltage in the faulty circuit. Eq. (3.18) can also be derived by taking the difference between the Kirchhoff's current law equations at node 1 for the faulted circuit and the unfaulted circuit (nominal).

Note that we have not as yet specified the port constraints in the circuit under test. In order to solve for the unknown admittance deviations from their nominal values, we need to measure the branch voltages $(V_{k+} \Delta V_k)^{(j)}$ for n independent test conditions. Thus, the superscript j denotes a particular test. We write

$$\begin{bmatrix} (V_{1+} \Delta V_1)^{(1)} & \cdots & (V_{n+} \Delta V_n)^{(1)} \\ \vdots & & \vdots \\ (V_{1+} \Delta V_1)^{(n)} & \cdots & (V_{n+} \Delta V_n)^{(n)} \end{bmatrix} \begin{bmatrix} \Delta Y_1 \\ \vdots \\ \Delta Y_n \end{bmatrix} = \begin{bmatrix} -\sum_{k=1}^{n} Y_{k0}\, \Delta V_k^{(1)} \\ \vdots \\ -\sum_{k=1}^{n} Y_{k0}\, \Delta V_k^{(n)} \end{bmatrix} \qquad \ldots(3.19)$$

For now, we assume that each of these tests is made at the same frequency. In order to obtain a unique solution to Eq. (3.19), the square branch voltage array must have rank n, that is, the rows of this square array must be independent. The necessary and sufficient test condition required to determine the admittances Y_1 through Y_n from branch voltage measurements can be found from the short-circuit admittance equations for the circuit.

$$Y\, \underline{V}_p = \underline{I}_p \qquad \ldots(3.20)$$

where the port voltages for a particular input excitation $\underline{I}_p^{(j)}$ is

$$\underline{V}_p^{(j)} = Y^{-1}\,\underline{I}_p^{(j)} \qquad \ldots(3.21)$$

Thus, in order to generate n independent port voltage vectors $\underline{V}_p^{(j)}$, $j=1,2,\ldots\ldots,n$, and hence, n independent branch voltage vectors $\underline{V}^{(j)}$, we need to excite the circuit with n independent current source vectors. One possible set of test conditions is given below.

Test Conditions: Set $I_{pj}= 1A$, and $I_{pi}= 0$, $i=1,2,\ldots.,n$, but $i\neq j$, and measure the branch voltages $(V_k+ \Delta V_k)^{(j)}$. Do this for $j=1,2,\ldots\ldots,n$, Figure 3.3. Substitute this information into Eq. (3.19) and solve for $\Delta\ Y_k, k=1,2,\ldots\ldots,n$.

Thus, the use of Tellegen's theorem and the concept of the adjoint circuit leads to a simple linear relationship between the unknown parameter changes and the branch voltage measurements. The number of linear algebraic equations which must be solved is equal to the number of unknown admittances connected to the node. Note also that the necessary and sufficient conditions for the determination of the admittances Y_1 through Y_n from only their branch voltages is that nodes 1 through n+1 be accessible. Finally, the above results apply not only to a collection of admittances connected to a common node, but also to any cutset of admittances in the circuit. Below a simple algorithm is given for the calculation of the admittances in a ladder network from node voltage measurements.

3.3 LADDER STRUCTURE NETWORKS

The ladder circuit is an important structure to consider since most passive filters (including mechanical and crystal filters) have the ladder structure.Also, many A/D and D/A converters contain a resistive

ladder network.In this section it will be shown that all the admittances in the arms of the ladder circuit can be uniquely determined from a simple matrix inversion.

Consider the ladder network in Figure 3.5.The following theorem states the minimum test conditions that are both necessary and sufficient to determine all the admittances from only voltage measurements at a single frequency.

Theorem

All the parameters in the ladder circuit can be uniquely determined from voltage measurements at a single frequency under the following two test conditions:

1) $I_{p1} \neq 0$, $I_{p2} = 0$ and measure the branch voltages $(V_i + \Delta V_i)^{(1)}$, $i=1,2,.....,2n+1$.

2) $I_{p1} = 0$, $I_{p2} \neq 0$ and measure the branch voltages $(V_i + \Delta V_i)^{(2)}$, $i=1,2,.....,2n+1$, and provided that

a) the circuit does not have transmission zeros at the measurement frequency, b) the series arm impedance $Z_{2k} \neq 0$ at the measurement frequency, and c) the equivalent impedance at any node in the circuit is finite.

Condition a) is necessary so that we have nonzero branch voltages to measure at the given test frequency, and b) is necessary in order to avoid having Y_{2k-1} and Y_{2k+1} in parallel at the test frequency.The admittances of parallel elements usually cannot be determined from only voltage measurements at a single frequency. Finally, in practice accuracy requirements may dictate that we perform more than the above number of minimum tests.Next, a proof is given for this theorem.

In order to simplify both the proof and the computational

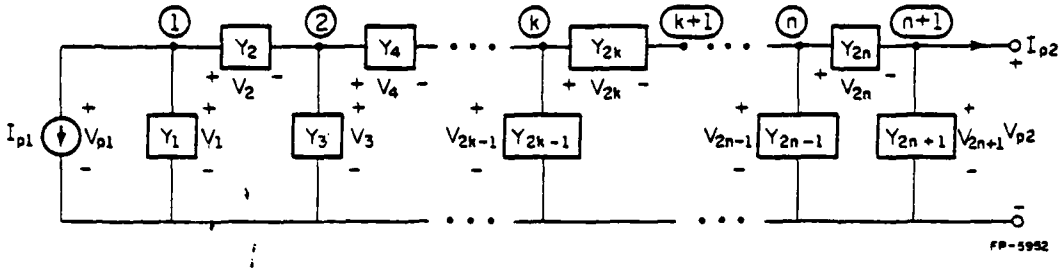


Fig. 3.5 Ladder network.

complexity of the method, we will isolate the elements at a single node by shorting the other nodes in the adjoint circuit and applying a 1A source at the non-shorted node as shown in Figure 3.6.We do this successively for all (n+1) nodes in the adjoint circuit. The first adjoint circuit isolates the admittances Y_1 and Y_2.The second adjoint circuit isolates the admittances Y_2,Y_3, and Y_4,etc. The last adjoint circuit ((n+1)th) isolates the admittances Y_{2n} and Y_{2n+1}.Then Eq. (3.19) becomes

$$\begin{bmatrix} (V_1+\Delta V_1)^{(1)}(V_2+\Delta V_2)^{(1)} & 0 & 0 & \cdots & 0 \\ (V_1+\Delta V_1)^{(2)}(V_2+\Delta V_2)^{(2)} & 0 & 0 & \cdots & 0 \\ 0 & -(V_2+\Delta V_2)^{(1)}(V_3+\Delta V_3)^{(1)} & (V_4+\Delta V_4)^{(1)} & \cdots & 0 \\ 0 & -(V_2+\Delta V_2)^{(2)}(V_3+\Delta V_3)^{(2)} & (V_4+\Delta V_4)^{(2)} & \cdots & 0 \\ 0 & 0 & 0 & -(V_4+\Delta V_4)^{(1)}\cdots & 0 \\ \cdot & \cdot & \cdot & & \cdot \\ \cdot & \cdot & \cdot & & \cdot \\ 0 & 0 & 0 & \cdots(V_{2n+1}+\Delta V_{2n+1})^{(1)} & \end{bmatrix} \begin{bmatrix} \Delta Y_1 \\ \Delta Y_2 \\ \Delta Y_3 \\ \Delta Y_4 \\ \cdot \\ \cdot \\ \cdot \\ \Delta Y_{2n+1} \end{bmatrix}$$

$$= \begin{bmatrix} -\Delta V_1^{(1)}Y_{1o}-\Delta V_2^{(1)}Y_{2o} \\ -\Delta V_1^{(2)}Y_{1o}-\Delta V_2^{(2)}Y_{2o} \\ \Delta V_2^{(1)}Y_{2o}-\Delta V_3^{(1)}Y_{3o}-\Delta V_4^{(1)}Y_{4o} \\ \Delta V_2^{(2)}Y_{2o}-\Delta V_3^{(2)}Y_{3o}-\Delta V_4^{(2)}Y_{4o} \\ \cdot \\ \cdot \\ \Delta V_{2n}^{(1)}Y_{2n,o}-\Delta V_{2n+1}^{(1)}Y_{2n+1,o} \end{bmatrix} \qquad \ldots(3.22)$$

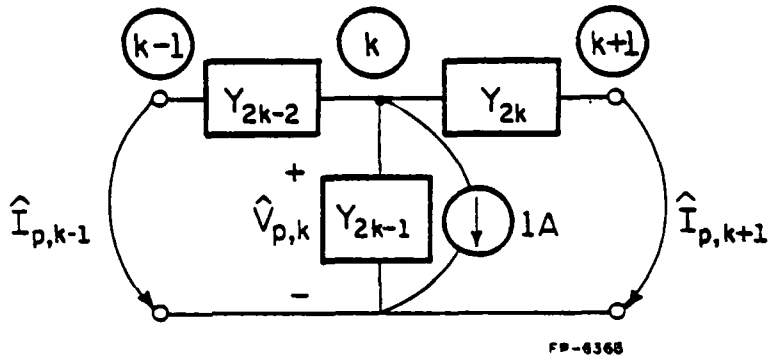


Fig. 3.6 Isolation of elements by shorting nodes in the adjoint circuit.

Solving the first two equations, we can determine ΔY_1 and ΔY_2.Then ΔY_2 is substituted for in both the third and fourth equations , which upon solving them we can determine ΔY_3 and ΔY_4.By proceeding in this manner, we can determine the unknowns ΔY_i, i=1,2,.....,2n+1.It is clear that we only solve subsystems of dimension 2x2 at most. Note that the last subsystem will have a dimension of 1x1.In this case, it is easy to see that the number of operations required to solve system (22) will be proportional to the dimension of the system.While if the matrix of Eq. (3.22) is full, then, the number of operations needed will be proportional to the dimension raised to the power of 3. This indicates that great saving in the computation effort will be achieved through the special choice of the adjoint circuits.

The proof of the last theorem will be based on studying the two equations resulting from the kth adjoint circuit; they are

$$\begin{bmatrix} -(V_{2k-2}+\Delta V_{2k-2})^{(1)} & (V_{2k-1}+\Delta V_{2k-1})^{(1)} & (V_{2k}+\Delta V_{2k})^{(1)} \\ -(V_{2k-2}+\Delta V_{2k-2})^{(2)} & (V_{2k-1}+\Delta V_{2k-1})^{(2)} & (V_{2k}+\Delta V_{2k})^{(2)} \end{bmatrix} \begin{bmatrix} \Delta Y_{2k-2} \\ \Delta Y_{2k-1} \\ \Delta Y_{2k} \end{bmatrix}$$

$$= \begin{bmatrix} \Delta V_{2k-2}{}^{(1)} Y_{2k-2} - \Delta V_{2k-1}{}^{(1)} Y_{2k-1} - \Delta V_{2k}{}^{(1)} Y_{2k} \\ \Delta V_{2k-2}{}^{(2)} Y_{2k-2} - \Delta V_{2k-1}{}^{(2)} Y_{2k-1} - \Delta V_{2k}{}^{(2)} Y_{2k} \end{bmatrix} \qquad \ldots(3.23)$$

In Eq. (3.23) there are only two unknowns, ΔY_{2k-1} and ΔY_{2k}.The ΔY_{2k-2} is determined in the (k-1)th solution.A necessary and sufficient condition to obtain a unique solution for the ΔY's is that

$$\frac{(V_{2k}+\Delta V_{2k})^{(1)}}{(V_{2k-1}+\Delta V_{2k-1})^{(1)}} \neq \frac{(V_{2k}+\Delta V_{2k})^{(2)}}{(V_{2k-1}+\Delta V_{2k-1})^{(2)}} \qquad ...(3.24)$$

The requirement that there be no transmission zeros at the measurement frequency insures that the above voltages are not zero.Also, Eq. (3.24) is equivalent to the requirement that

$$\frac{Z_{2k}}{Z_{2k}+\hat{Z}_{2k+1}} \neq \frac{-Z_{2k}}{\hat{Z}_{2k-1}} \qquad ...(3.25)$$

where $\hat{Z}_{2k-1}$ is the equivalent impedance at node k with $Y_{2k} = 0$, and $\hat{Z}_{2k+1}$ is the equivalent impedance at node k+1 with $Y_{2k}= 0$.We can write (25) as

$$Z_{2k}[Z_{2k}+\hat{Z}_{2k+1}+\hat{Z}_{2k-1}] \neq 0 \qquad ...(3.26)$$

Note that the equivalent impedance at the kth node is

$$Z_{eq,k} = \frac{\hat{Z}_{2k-1}[Z_{2k}+\hat{Z}_{2k+1}]}{Z_{2k}+\hat{Z}_{2k+1}+\hat{Z}_{2k-1}} \qquad ...(3.27)$$

This condition requires that $Z_{2k} \neq 0$ and that the equivalent impedance at each node be finite at the measurement frequency.The requirement that the voltages not be zero at the measurement frequency also means that there are no transmission zeros at the measurement frequency, that is Z_{2k} must be finite and $Z_{eq,k} \neq 0$ at this frequency.

In conclusion, this theorem gives two simple conditions by which all the impedances in a ladder network can be computed provided that the test frequency is not at any of the transmission zero frequencies, nor

is any of the series arm impedances zero at the test frequency. In the next section, we examine the possibility of using multiple test frequencies to determine the components in a circuit.

3.4 MULTIPLE TEST FREQUENCIES

Recall that in order to uniquely determine the admittance changes in a faulty circuit, we need to have n test conditions such that the rank of the square matrix in (19) is n, that is equal to the number of unknowns.In addition to exciting the circuit at different test points , we can also use different test frequencies; however, the admittances are frequency dependent in dynamic circuits.Thus, Eq. (3.19) must be written in terms of individual component changes, that is,

$$\begin{bmatrix} (j\omega_1)^{\alpha_1}(V_1+\Delta V_1)^{(1)} \ldots (j\omega_1)^{\alpha_n}(V_n+\Delta V_n)^{(1)} \\ \vdots \qquad\qquad \vdots \\ (j\omega_n)^{\alpha_1}(V_1+\Delta V_1)^{(n)} \ldots (j\omega_n)^{\alpha_n}(V_n+\Delta V_n)^{(n)} \end{bmatrix} \begin{bmatrix} \Delta P_1 \\ \vdots \\ \Delta P_n \end{bmatrix}$$

$$= \begin{bmatrix} -\sum_{k=1}^{n} Y_{ko}(j\omega_1)\Delta V_k^{(1)} \\ \vdots \\ -\sum_{k=1}^{n} Y_{ko}(j\omega_n)\Delta V_k^{(n)} \end{bmatrix} \qquad \ldots(3.28)$$

where $\Delta P_j = \Delta G_j$, ΔC_j, or $\Delta \Gamma_j$ and the exponent $\alpha_j = 0, +1$, or -1, depending

on if the jth branch is a resistor, capacitor, or inductor, respectively.The voltage $(V_j+\Delta V_j)^{(i)}$ is measured at the frequency ω_i.

If we assume a single unit input function and that the branch voltage is a rational function of the complex frequency s, then we can write (28) as (without any pole-zero cancellation)

$$\text{diag}\left[\frac{1}{D(s_1)} \cdots \frac{1}{D(s_n)}\right]\begin{bmatrix} s_1^{\alpha_1}N_1(s_1) & \cdots & s_1^{\alpha_n}N_n(s_1) \\ \vdots & & \vdots \\ s_n^{\alpha_1}N_1(s_n) & \cdots & s_n^{\alpha_n}N_n(s_n) \end{bmatrix}\begin{bmatrix} \Delta P_1 \\ \vdots \\ \Delta P_n \end{bmatrix}$$

$$= \begin{bmatrix} -\sum_{k=1}^{n} Y_{ko}(s_1)\Delta V_k^{(1)} \\ \vdots \\ -\sum_{k=1}^{n} Y_{ko}(s_n)\Delta V_k^{(n)} \end{bmatrix} \qquad \ldots(3.29)$$

where the polynomial D(s) yields the poles of the transfer function for the branch voltages with respect to the input port, and $N_i(s)$ yields the zeros.A necessary and sufficient condition for the solution of Eq. (3.29) is that the square matrix on the left is nonsingular.This means that none of the test frequencies can be a pole of the polynomial D(s) (in case there are pure imaginary poles).Also, the circuit cannot have two identical element types in parallel.Note that the above matrix can be written in the form

$$\begin{bmatrix} s_1^{\alpha_1}N_1(s_1)\ldots s_1^{\alpha_n}N_n(s_1) \\ \vdots \\ s_n^{\alpha_1}N_1(s_n)\ldots s_n^{\alpha_n}N_n(s_n) \end{bmatrix} = \begin{bmatrix} \sum_{i=0}^{n-1} a_i(1)s_1^i \ldots \sum_{i=0}^{n-1} a_i(n)s_1^i \\ \vdots \\ \sum_{i=0}^{n-1} a_i(1)s_n^i \ldots \sum_{i=0}^{n-1} a_i(n)s_1^i \end{bmatrix} = S\ A \quad \ldots(3.30)$$

where S and A are nxn matrices given by

$$S = \begin{bmatrix} 1 & s_1 & s_1^2 \ldots & s_1^{n-1} \\ 1 & s_2 & s_2^2 \ldots & s_2^{n-1} \\ \vdots & & & \\ 1 & s_n & s_n^2 \ldots & s_n^{n-1} \end{bmatrix} \quad .(3.31\text{-a})$$

$$A = \begin{bmatrix} a_0(1) & a_0(2) \ldots & a_0(n) \\ a_1(1) & a_1(2) \ldots & a_1(n) \\ \vdots & & \\ a_{n-1}(1) & a_{n-1}(2) \ldots & a_{n-1}(n) \end{bmatrix} \quad .(3.31\text{-b})$$

Then, a necessary and sufficient condition for the solution of Eq. (29) is that both matrices S and A be nonsingular.This implies that the n test frequencies should be different pairwise.Also, the difference between the highest degree and lowest degree terms of at least one of the polynomials $s^{\alpha_i}N_i(s)$ in Eq. (3.29) be n-1, to insure that there will be no zero row in the coefficient matrix A.In addition, the coefficient matrix A is of full rank.

If these necessary and sufficient conditions are satisfied, then,

one can always find a set of n frequencies such that the rank of the square matrix in Eq. (3.29) is n.

Note that by using different measurement frequencies, we can determine the value of different types of parallel elements, while this is impossible under only single frequency voltage measurements.Below an alternative algorithm is given for the calculation of the impedances in dynamic ladder circuits with different type elements.

3.5 LADDER NETWORKS

Consider the same ladder network as before, Figure 3.5, where the structure has different type elements. Recall that in order to uniquely determine all the parameters, we need two test conditions.The first test consists of exciting port 1 with a current source and measuring all branch voltages, while in the second test port 2 is excited with a current source and all the branch voltages are measured.These two test conditions are performed at the same frequency.

In this section, we will show that we can also uniquely determine all the parameters of a ladder circuit from the following two test conditions.

Test Conditions:

1) With $I_{p1}\neq 0$ and $I_{p2}=0$ measure all the branch voltages $(V_i+\Delta V_i)^{(1)}, i=1,2,.....,2n+1$ at the frequency f_1.

2) With $I_{p1}\neq 0$ and $I_{p2}=0$ measure all the branch voltages $(V_i+\Delta V_i)^{(2)}, i=1,2,.....,2n+1$ at the frequency f_2.

These test conditions together with the same adjoint circuits will yield the following linear system of equations.

$$
\begin{bmatrix}
(j\omega_1)^{\alpha_1}(V_1+\Delta V_1)^{(1)} & (j\omega_1)^{\alpha_2}(V_2+\Delta V_2)^{(1)} & 0 & 0 & \cdots & 0 \\
(j\omega_2)^{\alpha_1}(V_1+\Delta V_1)^{(2)} & (j\omega_2)^{\alpha_2}(V_2+\Delta V_2)^{(2)} & 0 & 0 & \cdots & 0 \\
0 & -(j\omega_1)^{\alpha_2}(V_2+\Delta V_2)^{(1)} & (j\omega_1)^{\alpha_3}(V_3+\Delta V_3)^{(1)} & (j\omega_1)^{\alpha_4}(V_4+\Delta V_4)^{(1)} & \cdots & 0 \\
0 & -(j\omega_2)^{\alpha_2}(V_2+\Delta V_2)^{(2)} & (j\omega_2)^{\alpha_3}(V_3+\Delta V_3)^{(2)} & (j\omega_2)^{\alpha_4}(V_4+\Delta V_4)^{(2)} & \cdots & 0 \\
\cdot & \cdot & \cdot & \cdot & & \cdot \\
\cdot & \cdot & \cdot & \cdot & & \cdot \\
0 & 0 & 0 & 0 & \cdots & (j\omega_1)^{\alpha_{2n+1}}(V_{2n+1}+\Delta V_{2n+1})^{(1)}
\end{bmatrix}
\begin{bmatrix} \Delta P_1 \\ \Delta P_2 \\ \Delta P_3 \\ \Delta P_4 \\ \cdot \\ \cdot \\ \Delta P_{2n+1} \end{bmatrix}
$$

$$
= \begin{bmatrix}
-\Delta V_1^{(1)} Y_{1o}(j\omega_1) - \Delta V_2^{(1)} Y_{2o}(j\omega_1) \\
-\Delta V_1^{(2)} Y_{1o}(j\omega_2) - \Delta V_2^{(2)} Y_{2o}(j\omega_2) \\
\Delta V_2^{(1)} Y_{2o}(j\omega_1) - \Delta V_3^{(1)} Y_{3o}(j\omega_1) - \Delta V_4^{(1)} Y_{4o}(j\omega_1) \\
\Delta V_2^{(2)} Y_{2o}(j\omega_2) - \Delta V_3^{(2)} Y_{3o}(j\omega_2) - \Delta V_4^{(2)} Y_{4o}(j\omega_2) \\
\cdot \\
\cdot \\
\Delta V_{2n}^{(1)} Y_{2n,o}(j\omega_1) - \Delta V_{2n+1}^{(1)} Y_{2n+1,o}(j\omega_1)
\end{bmatrix} \quad \ldots(3.32)
$$

where $\Delta P_j = \Delta G_j$, ΔC_j, or $\Delta \Gamma_j$ and the exponent $\alpha_j = 0, +1$, or -1 depending on if the jth branch is a resistor, capacitor, or inductor, respectively. As stated before, solving the linear system (32) will be very computationally efficient, because in each step, we solve only a 2x2 linear subsystem, except the last one has a dimension of 1 .

In this case, a necessary and sufficient condition for the solution of Eq. (3.32) is that each 2x2 submatrix and the last 1x1 submatrix be nonsingular. Consider the two equations resulting from the kth adjoint circuit, they are (after some manipulation)

$$\begin{bmatrix} (j\omega_1)^{\alpha_{2k-1}} (V_{2k-1}+\Delta V_{2k-1})^{(1)} & (j\omega_1)^{\alpha_{2k}} (V_{2k}+\Delta V_{2k})^{(1)} \\ (j\omega_2)^{\alpha_{2k-1}} (V_{2k-1}+\Delta V_{2k-1})^{(2)} & (j\omega_2)^{\alpha_{2k}} (V_{2k}+\Delta V_{2k})^{(2)} \end{bmatrix} \begin{bmatrix} \Delta P_{2k-1} \\ \Delta P_{2k} \end{bmatrix}$$

$$= \begin{bmatrix} \Delta e_{2k-1}^{(1)} \\ \Delta e_{2k}^{(2)} \end{bmatrix} \qquad \ldots(3.33)$$

A necessary and sufficient condition to obtain a unique solution for ΔP_{2k-1} and ΔP_{2k} is that

$$(j\omega_1)^{\alpha_d} \frac{(V_{2k-1}+\Delta V_{2k-1})^{(1)}}{(V_{2k}+\Delta V_{2k})^{(1)}} \neq (j\omega_2)^{\alpha_d} \frac{(V_{2k-1}+\Delta V_{2k-1})^{(2)}}{(V_{2k}+\Delta V_{2k})^{(2)}} \qquad \ldots(3.34)$$

where, $\alpha_d = \alpha_{2k-1} - \alpha_{2k}$ $\qquad \ldots(3.35)$

and can have an integer value in [-2,+2].

This implies that there be no transmission zeros at the measurement frequencies, to insure that the above voltages are not zero. Also, the two frequencies must be different. In addition, the series arm $Z_{2k} \neq 0$,

and the equivalent impedance at any node of the circuit should be finite at both of the measurement frequencies, otherwise we get a zero determinant. Note that the only way that Eq. (3.34) is not satisfied, is when we have either a circuit with the same element type structure, or the complex function F(s) has the same value at two different frequencies, where

$$F(s)=(s)^{\alpha_d}\ \frac{(V_{2k-1}(s)+\Delta V_{2k-1}(s))}{(V_{2k}(s)+\Delta V_{2k}(s))} \qquad \ldots(3.36)$$

Obviously, we exclude circuits with structures of the same element type.

With the above conditions satisfied, one can always find two different frequencies such that Eq. (3.34) is satisfied, which means that the matrix of Eq. (3.33) is nonsingular.

3.6 MIXED TEST CONDITIONS

So far, we have shown that in order to isolate a group of n elements in a cut set of a circuit, we need n different test conditions such that the matrix of Eq. (3.19) is nonsingular.These n different test conditions could be obtained through two ways.First, by exciting n specified ports with a current source at the same frequency and measuring branch voltages.Second, by exciting one specified port at n specified frequencies, and also measuring branch voltages.Using the second way, we can determine the value of different type parallel elements, which is not possible through the first way.On the other hand, using the first way, we can handle single element type structures, which is not possible through the second way.

Sometimes it is necessary to use a combination of the above test

conditions in order to uniquely determine the element values.In other words, we can excite our circuit at different ports with different frequency current sources.This approach would be needed in circuits where there is at least a group of different type elements connected in parallel, etc.

As an example to illustrate this, consider the circuit shown in Figure 3.7, where we need to determine the parameter deviations in R_1,R_2,L,and C.The test conditions for this circuit will be

Test Conditions:

1) Connect a current source between nodes a and o, and measure $(V_1+\Delta V_1)^{(i)}$ and $(V_2+\Delta V_2)^{(i)}$ at three different frequencies f_i, i=1,2,3.

2) Connect a current source between nodes b and o, and measure $(V_1+\Delta V_1)^{(4)}$ and $(V_2+\Delta V_2)^{(4)}$ at one frequency, say f_1.

Under these test conditions, we will have

$$\begin{bmatrix} s_1^{-1}(V_1+\Delta V_1)^{(1)} & s_1(V_1+\Delta V_1)^{(1)} & (V_1+\Delta V_1)^{(1)} & (V_2+\Delta V_2)^{(1)} \\ s_2^{-1}(V_1+\Delta V_1)^{(2)} & s_2(V_1+\Delta V_1)^{(2)} & (V_1+\Delta V_1)^{(2)} & (V_2+\Delta V_2)^{(2)} \\ s_3^{-1}(V_1+\Delta V_1)^{(3)} & s_3(V_1+\Delta V_1)^{(3)} & (V_1+\Delta V_1)^{(3)} & (V_2+\Delta V_2)^{(3)} \\ s_1^{-1}(V_1+\Delta V_1)^{(4)} & s_1(V_1+\Delta V_1)^{(4)} & (V_1+\Delta V_1)^{(4)} & (V_2+\Delta V_2)^{(4)} \end{bmatrix} \begin{bmatrix} \Delta\Gamma \\ \Delta C \\ \Delta G_1 \\ \Delta G_2 \end{bmatrix}$$

$$= \begin{bmatrix} -(s_1^{-1}L_o^{-1}+s_1C_o+G_{1o})\Delta V_1^{(1)}-G_{2o}\Delta V_2^{(1)} \\ -(s_2^{-1}L_o^{-1}+s_2C_o+G_{1o})\Delta V_1^{(2)}-G_{2o}\Delta V_2^{(2)} \\ -(s_3^{-1}L_o^{-1}+s_3C_o+G_{1o})\Delta V_1^{(3)}-G_{2o}\Delta V_2^{(3)} \\ -(s_1^{-1}L_o^{-1}+s_1C_o+G_{1o})\Delta V_1^{(4)}-G_{2o}\Delta V_2^{(4)} \end{bmatrix} \qquad \ldots(3.37)$$

Solving Eq.(37), we can determine the deviation in parameters $\Delta\Gamma$, ΔC, ΔG_1, and ΔG_2.

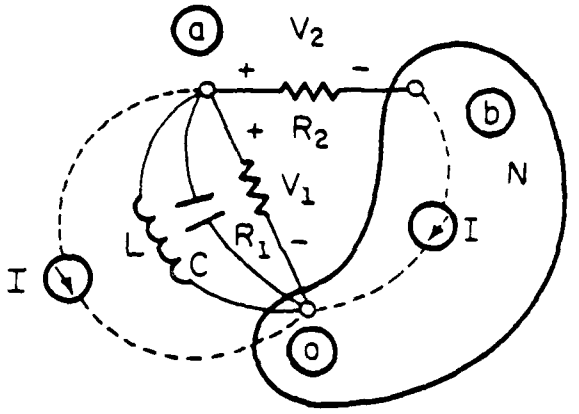


Fig. 3.7 Calculation of RLC parallel elements.

In the next section, the effect of measurement errors on the solution for parameter deviations will be studied.In addition, the dependence of that solution on the first-order sensitivities of the circuit will be revealed.

3.7 EFFECT OF MEASUREMENT ERRORS ON THE SOLUTION

It has been shown that, in order to isolate the group of n elements in Figure 3.3, we need to solve the nxn linear nonsingular system of Eq. (3.19) or Eq. (3.28).Any of these systems is constructed mainly from voltage measurements. Practically, voltage measurements are obtained within some tolerance depending on the accuracy of the measuring device.

In order to examine the effect of these measurement errors on the solution, we will apply the perturbation theory [18,19] on our linear system.

3.7.1 ERROR ANALYSIS IN LINEAR SYSTEMS

Any of the linear systems given by Eqs. (3.19) or (3.28) could be rewritten as

$$A\,\underline{x} = \underline{b} \qquad \ldots(3.38)$$

where A in an nxn nonsingular matrix and its entries are measured voltages under different test conditions, $\underline{x}$ is the unknown parameter deviations vector, and $\underline{b}$ is the right-hand side vector, where its entries also depend upon the measured voltages.Having errors in the measured voltages is like perturbing both A and $\underline{b}$, simultaneously. Then, the problem of studying the effect of measurement errors on the

solution will be equivalent to the problem of studying the effect of perturbations in both A and $\underline{b}$ on the solution $\underline{x}$ in Eq. (3.38). Incidently, the problem of studying the effect of perturbations in A and $\underline{b}$ individually on $\underline{x}$ was done in [18,19].Upper bounds on the resulting relative error in $\underline{x}$ were derived in each case.Next, we will obtain an upper bound on the relative error in $\underline{x}$ resulting from simultaneous perturbation in both A and $\underline{b}$.

3.7.1.1 EFFECT OF PERTURBATIONS IN $\underline{b}$ ON $\underline{x}$

In this section, we will consider the effect of perturbations only in the right-hand side vector $\underline{b}$ on the solution vector $\underline{x}$ of Eq. (3.38). Specifically, we assume that only $\underline{b}$ is perturbed to $\underline{b}+\delta\underline{b}$, while A is held fixed.Consequently, $\underline{x}$ will be perturbed to $\underline{x}+\delta\underline{x}_b$, and Eq.(38) becomes

$$A(\underline{x}+\delta\underline{x}_b) = \underline{b}+\delta\underline{b} \qquad \ldots(3.39)$$

Subtracting Eq. (3.38) from Eq. (3.39), we get

$$A\,\delta\underline{x}_b = \delta\underline{b} \qquad \ldots(3.40)$$

or

$$\delta\underline{x}_b = A^{-1}\,\delta\underline{b} \qquad \ldots(3.41)$$

By taking norms of both sides

$$\|\delta \underline{x}_b\| \leq \|A^{-1}\| \ \|\delta \underline{b}\|^{*} \qquad \ldots(3.42)$$

Also, taking norms of both sides of Eq. (3.38)

$$\|\underline{b}\| \leq \|A\| \ \|\underline{x}\| \qquad \ldots(3.43)$$

Multiplying Eqs. (3.42) and (3.43), we get

$$\|\delta \underline{x}_b\| \ \|\underline{b}\| \leq \|A\| \ \|A^{-1}\| \ \|\underline{x}\| \ \|\delta \underline{b}\| \qquad \ldots(3.44)$$

Assuming that $\underline{b} \neq 0$, we get

$$\frac{\|\delta \underline{x}_b\|}{\|\underline{x}\|} \leq \text{Cond}(A) \frac{\|\delta \underline{b}\|}{\|\underline{b}\|} \qquad \ldots(3.45)$$

where $\text{Cond}(A) = \|A\| \ \|A^{-1}\| = (\mu_1 / \mu_n) \geq 1$ ...(3.46)

and μ_1 and μ_n are the largest and smallest singular values of matrix A, respectively, i.e., μ_1^2 and μ_n^2 are the largest and smallest eigenvalues of $\overline{A}^T A$, respectively, where $\overline{A}^T$ is the complex conjugate transposed of A.

Eq. (3.45) is an expression for the upper bound on the relative error in $\underline{x}$ due to perturbation in $\underline{b}$.Note that the quantity Cond(A), named as the condition of matrix A, appears in that upper bound and it has a minimum value of unity.

(*) If $\underline{x} = [x_1, x_2, \ldots, x_n]^T$ is a vector of n components, we mean by $\|\underline{x}\| = [|x_1|^2 + |x_2|^2 + \ldots + |x_n|^2]^{0.5}$. If B in an nxn matrix, we mean by $\|B\| = \max(\|B\underline{x}\| / \|\underline{x}\|)$ over $\|\underline{x}\| \neq 0$.

3.7.1.2 EFFECT OF PERTURBATIONS IN A ON $\underline{x}$

In this section, we will consider the effect of perturbations only in the matrix A on the solution vector $\underline{x}$ of Eq. (3.38).In particular, we assume that only A is perturbed to A+δA, while $\underline{b}$ is fixed.Accordingly, $\underline{x}$ will be perturbed to $\underline{x}+\delta\underline{x}_A$, and Eq. (3.38) becomes

$$(A+\delta A)(\underline{x}+\delta\underline{x}_A) = \underline{b} \qquad \ldots(3.47)$$

Subtracting Eq. (3.38) from Eq. (3.47), we get

$$(A+\delta A)\ \delta\underline{x}_A = -\delta A\ \underline{x} \qquad \ldots(3.48)$$

Assuming $\|A^{-1}\ \delta A\| < 1$, then, (A+δA) is nonsingular, and we will have

$$\delta\underline{x}_A = -(I+A^{-1}\delta A)^{-1}\ A^{-1}\ \delta A\ \underline{x} \qquad \ldots(3.49)$$

By taking norms of both sides, we get

$$\frac{\|\delta\underline{x}_A\|}{\|\underline{x}\|} \leq \|(I+A^{-1}\delta A)^{-1}\|\ \|A^{-1}\delta A\|$$

$$\leq \frac{\|A^{-1}\delta A\|}{1-\|A^{-1}\delta A\|}\ (**)$$

$$\leq \frac{\|A^{-1}\|\ \|\delta A\|}{1-\|A^{-1}\|\ \|\delta A\|} \qquad \ldots(3.50)$$

which could be rewritten as

$$\frac{\|\delta \underline{x}_A\|}{\|\underline{x}\|} \leq \frac{\text{Cond}(A)[\|\delta A\|/\|A\|]}{1-\text{Cond}(A)[\|\delta A\|/\|A\|]} \qquad \ldots(3.51)$$

which is the upper bound on the relative error in $\underline{x}$ due to perturbations in A. Note that the quantity Cond(A) appears also in this upper bound.

3.7.1.3 EFFECT OF PERTURBATIONS IN A AND $\underline{b}$ ON $\underline{x}$

In this section, we will consider the effect of simultaneous perturbations in both the matrix A and the right-hand side vector $\underline{b}$ on the solution vector $\underline{x}$ of Eq. (3.38). This case is important because it will be the actual situation when we have errors in the voltage measurements, as shown before. Hence, assume that A is perturbed to $A+\delta A$, while $\underline{b}$ is perturbed to $\underline{b}+\delta\underline{b}$. Consequently, $\underline{x}$ will be perturbed to $\underline{x}+\delta\underline{x}$, and Eq. (3.38) becomes

$$(A+\delta A)(\underline{x}+\delta\underline{x}) = \underline{b}+\delta\underline{b} \qquad \ldots(3.52)$$

and our goal is to get a relation between $\delta\underline{x}$, and both of δA and $\delta\underline{b}$. Equivalently, we can get a relation between $\delta\underline{x}$ and both $\delta\underline{x}_A$ and $\delta\underline{x}_b$, where $\delta\underline{x}_A$ and $\delta\underline{x}_b$ are the perturbations in $\underline{x}$ due to individual perturbations in A and $\underline{b}$, respectively.

Subtracting Eq. (3.38) from Eq. (3.52), we get

(**) Since $I=(I+B)^{-1}(I+B)=(I+B)^{-1}+(I+B)^{-1}B$, hence, $1=\|I\| \geq \|(I+B)^{-1}\| - \|(I+B)^{-1}B\| \geq \|(I+B)^{-1}\| - \|(I+B)^{-1}\|\,\|B\|$, which reduces to $\|(I+B)^{-1}\| \leq 1/(1-\|B\|)$; provided that $\|B\| < 1$.

$$(A+\delta A)\,\underline{\delta x} = -\delta A\,\underline{x} + \underline{\delta b} \qquad \ldots(3.53)$$

Substitute from Eqs. (3.40) and (3.48) into (3.53)

$$(A+\delta A)\,\underline{\delta x} = (A+\delta A)\,\underline{\delta x}_A + A\,\underline{\delta x}_b \qquad \ldots(3.54)$$

Again, assume that $|A^{-1}\delta A| < 1$, then $(A+\delta A)$ is nonsingular

$$\underline{\delta x} = \underline{\delta x}_A + (I+A^{-1}\delta A)^{-1}\,\underline{\delta x}_b \qquad \ldots(3.55)$$

Take the norms of both sides, then divide both sides by $|\underline{x}|$

$$\frac{\|\underline{\delta x}\|}{\|\underline{x}\|} \leq \frac{\|\underline{\delta x}_A\|}{\|\underline{x}\|} + \frac{1}{1-\|A^{-1}\|\,\|\delta A\|}\,\frac{\|\underline{\delta x}_b\|}{\|\underline{x}\|} \qquad \ldots(3.56)$$

Finally, substitute from (45) and (51) into (56)

$$\frac{\|\underline{\delta x}\|}{\|\underline{x}\|} \leq \frac{\mathrm{Cond}(A)}{1-\mathrm{Cond}(A)[\|\delta A\|/\|A\|]}\left(\frac{\|\delta A\|}{\|A\|} + \frac{\|\underline{\delta b}\|}{\|\underline{b}\|}\right) \qquad \ldots(3.57)$$

Eq. (3.57) is the expression for the upper bound on the relative error in $\underline{x}$ due to simultaneous error in both A and $\underline{b}$. As anticipated, Cond(A) appears in this expression.

In order to lessen the relative error in $\underline{x}$ due to errors in A and/or $\underline{b}$, it is necessary to push the upper bound(s) down as far as possible. One obvious way to keep relatively small upper bounds is by keeping small relative errors in A and $\underline{b}$, i.e. by keeping small errors in the measurements. Another way, is by having low values of Cond(A). Moreover , for certain values of relative errors in A and $\underline{b}$, the

relative error in $\underline{x}$ is minimum when Cond(A)=1. In general, knowing the value of Cond(A) together with the maximum relative error in A and $\underline{b}$, one can have a clear idea of the accuracy of the solution $\underline{x}$.

Note that the assumption $\|A^{-1}\| \|\delta A\| < 1$ used before is practically feasible, since the measurement errors are usually very small compared to exact values.

In the next section, we will apply the error analysis to the ladder structures and try to relate Cond(A) to the circuit specifications.

3.7.2 LADDER STRUCTURE NETWORKS

As shown above, in order to have an idea about the accuracy obtained when solving for the network parameter deviations, we need to examine the condition of the square matrix of the corresponding linear set of equations. Since in case of ladder structures, Figure 3.5, we will have linear subsystems of dimension at most 2x2. Then it is sufficient to study the condition of a 2x2 general submatrix in Eq. (3.22), where the A matrix is given by

$$A = \begin{bmatrix} (V_{2k-1}+\Delta V_{2k-1})^{(1)} & (V_{2k}+\Delta V_{2k})^{(1)} \\ (V_{2k-1}+\Delta V_{2k-1})^{(2)} & (V_{2k}+\Delta V_{2k})^{(2)} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \qquad \ldots(3.58)$$

For this 2x2 matrix, an analytic expression for Cond(A) is available in terms of a_{ij}, the entries of matrix A [18], which is

$$\text{Cond}(A) = \sigma + (\sigma^2 - 1)^{0.5} \qquad \ldots(3.59)$$

where,

$$\sigma = [|a_{11}|^2+|a_{12}|^2+|a_{21}|^2+|a_{22}|^2]/[2\,|a_{11}a_{22}-a_{12}a_{21}|] \qquad ...(3.60)$$

It is clear from Eq. (3.55) that Cond(A) is continuous monotone-increasing with σ on $[1,\infty)$. Hence, the lower value of σ, the smallest value of Cond(A), is the smallest relative error in the solution vector due to errors in the voltage measurements.

Under the previously specified two test conditions in the theorem, we will have the equivalent networks shown in Figures 3.8-a and 3.8-b. For simplicity, we assume that we have a network with elements of the same type. Without loss of generality, we assume that we adjust the excitations such that the Norton's equivalent current source is 1A in each in Figures 3.8-a and 3.8-b. Under these assumptions, we will have the following voltage expressions

$$V_{2k-1}^{(1)} = -\hat{Z}_{2k-1}(Z_{2k}+\hat{Z}_{2k+1})/(\hat{Z}_{2k-1}+Z_{2k}+\hat{Z}_{2k+1}) \qquad .(3.61\text{-a})$$

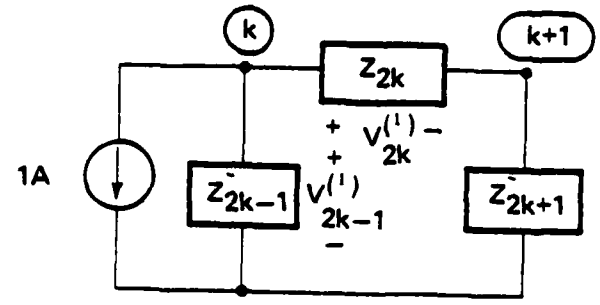
$$V_{2k}^{(1)} = -\hat{Z}_{2k-1}Z_{2k}/(\hat{Z}_{2k-1}+Z_{2k}+\hat{Z}_{2k+1}) \qquad .(3.61\text{-b})$$

$$V_{2k-1}^{(2)} = -Z_{2k-1}\hat{Z}_{2k+1}/(\hat{Z}_{2k-1}+Z_{2k}+\hat{Z}_{2k+1}) \qquad .(3.61\text{-c})$$

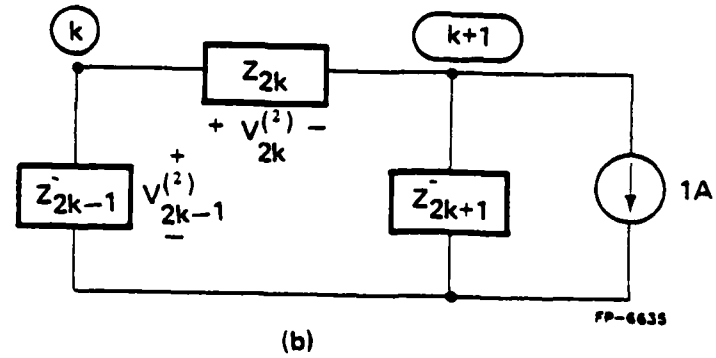
$$V_{2k}^{(2)} = -Z_{2k}\hat{Z}_{2k+1}/(\hat{Z}_{2k-1}+Z_{2k}+\hat{Z}_{2k+1}) \qquad .(3.61\text{-d})$$

Substituting from Eqs. (3.58) and (3.61) into (3.60), then, dividing both numerator and denominator of the resulting equation by $|\hat{Z}_{2k-1}|^2|\hat{Z}_{2k+1}|^2$, we get

$$\sigma = (\alpha^2+0.5\,\beta^2+\alpha+1)/(\alpha+\alpha\beta+\beta) \qquad ...(3.62)$$



(a)



(b)

Fig. 3.8 (a) Norton's equivalent circuit at nodes k and k+1 under the first test condition.
(b) Norton's equivalent circuit at nodes k and k+1 under the second test condition.

where α and β are impedance ratios, given by

$$\alpha = Z_{2k}/Z_{2k+1} \quad \text{,and} \quad \beta = Z_{2k}/Z_{2k-1} \qquad \ldots(3.63)$$

According to the previous theorem, α and β must be finite and non-zero. In addition, they are positive and real quantities due to the assumption of same element type structures. As stated before, we wish to have as low a value of σ as possible in order to have low relative error in the solution. In addition, the minimum value of σ is 1, which makes Cond(A) equal to 1, a minimum also.

A closer look at the function of Eq. (3.62) yields the following data

a) If $\alpha = \beta$, then $\sigma = (1.5\alpha^2 + \alpha + 1)/(\alpha^2 + \alpha)$. Hence, $\sigma \in [1.118, 1.5]$ for $\alpha \in [0.5, \infty)$, as shown in Figure 3.9.

b) $\alpha = 1$ and $\beta = 2$ gives a minimum value of σ, which is unity.

Hence, in order to have a low value of σ, α and β should not be small, and they should be close in value. This suggests that ladder networks, with nearly equal arm impedance values and equivalent impedance values at each node, will have very low relative error in the solution for the parameter deviations due to errors in the measurements. Examples of such structures, in practice, are A/D and D/A converters, etc.

For general topology networks, it is not easy to adopt the same analysis to extend the result obtained for ladder structures. This is because of the fact that it is not possible to get an analytic expression for the condition of matrices having dimensions higher than 2x2. Rather, we would draw a similar conclusion, but using the concept

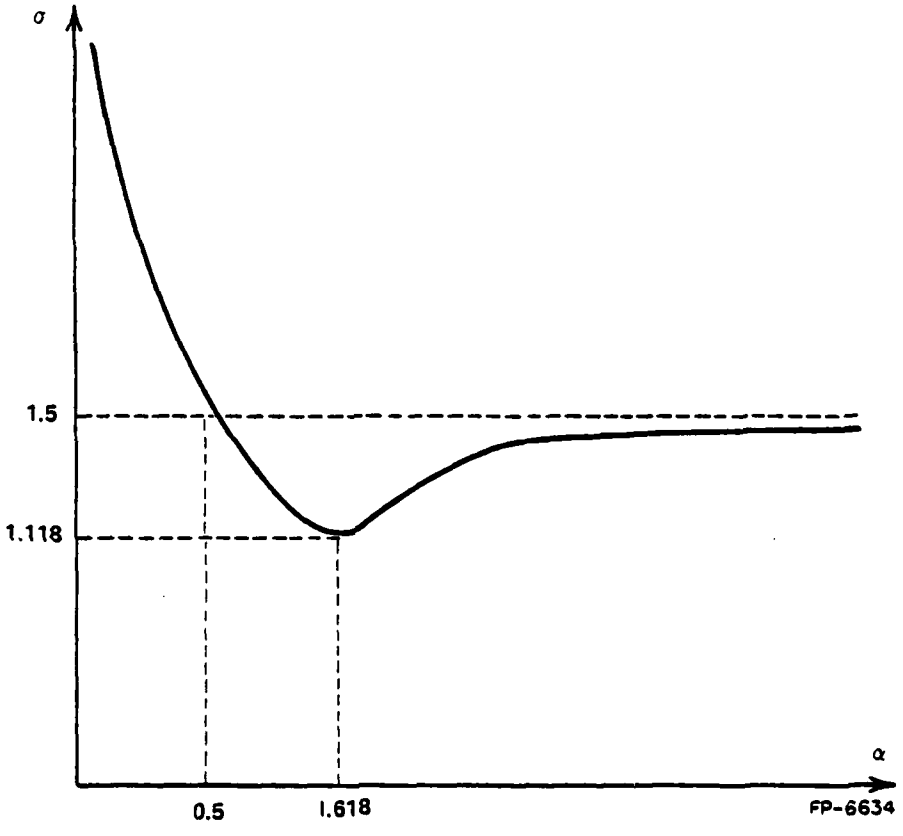


Fig. 3.9 Relation between σ and α when $\alpha = \beta$.

of first-order sensitivities.

Consider a general topology network as shown in Figure 3.10. Assume , for simplicity, that it is a linear passive circuit, and port 1 is the input port with voltage source as an excitation. Also, consider its adjoint circuit, Figure 3.11, where port 1 is shorted and port m (output port) is excited by a 1A current source. Then Eq. (3.14) becomes

$$\sum_{k=1}^{b} S_{Y_k}^{V_{pm}} \left(1+\frac{\Delta V_k}{V_k}\right) \frac{\Delta Y_k}{Y_k} = \frac{\Delta V_{pm}}{V_{pm}} \qquad \ldots(3.64)$$

By generating b independent equations of Eq. (3.64), we can solve for the ΔY_k's. In this case, it is also desirable that we have as low matrix condition value as possible. Now, suppose that the system matrix is transformed into a diagonalized form using orthogonal matrices. Then the matrix condition value will not be affected [18]. This will be equivalent to the following system. First, assume that we have a network N_1, that is the same as network N, but only element Y_1 has a fault ΔY_1. Second, assume that we have another network N_2, that is the same as network N, but only the element Y_2 has a fault ΔY_2. By doing so, we can generate the following equivalent system of equations.

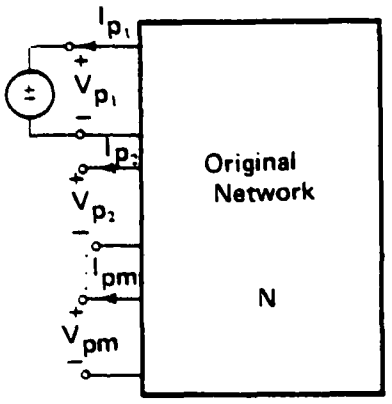


Fig. 3.10 Linear circuit with m ports.

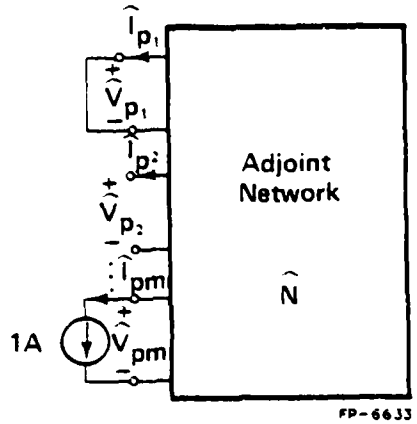


Fig. 3.11 Adjoint circuit of circuit under test.

$$\begin{bmatrix} S_{Y_1}^{V_{pm}} & 0 & \cdots & 0 \\ 0 & S_{Y_2}^{V_{pm}} & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & S_{Y_b}^{V_{pm}} \end{bmatrix} \begin{bmatrix} (1+\frac{\Delta V_1}{V_1})(1)\frac{\Delta Y_1}{Y_1} \\ (1+\frac{\Delta V_2}{V_2})(2)\frac{\Delta Y_2}{Y_2} \\ \vdots \\ (1+\frac{\Delta V_b}{V_b})(b)\frac{\Delta Y_b}{Y_b} \end{bmatrix} = \begin{bmatrix} \frac{\Delta V_{pm}^{(1)}}{V_{pm}} \\ \frac{\Delta V_{pm}^{(2)}}{V_{pm}} \\ \vdots \\ \frac{\Delta V_{pm}^{(b)}}{V_{pm}} \end{bmatrix} \quad \ldots(3.65)$$

This system is equivalent to the original system of equations because, it yields the same solution for the ΔY_k's. Then, for the diagonal matrix of Eq. (3.65) to have as low condition value as possible, we should have very close values for $S_{Y_k}^{V_{pm}}$; k=1,2,....,b. In other words, having very close values for the first-order sensitivities will help keep low matrix condition value, and consequently, low errors in the solution due to measurement errors.

Generally, it is a good idea that, during the course of solving for element deviations, one solves for the singular values for the different submatrices to determine their condition values. These values will give a good indication of the accuracy of the computed parameter deviations.

3.7.3 SOME PRACTICAL CONSIDERATIONS

It was shown in Eq. (3.22), that for ladder networks, we only need two test conditions. Moreover, the formulation allowed us to solve for two (or one) elements at a time, e.g., first we solve for ΔY_1 and ΔY_2, then using the obtained value for ΔY_2, we solve for ΔY_3 and ΔY_4. This is done repeatedly until we solve for all the element deviations. Depending on the element types and values, and the test frequency(s), one or more of the 2x2 submatrices in Eq. (3.22) may be

ill-conditioned. This will cause a numerical problem in obtaining the element deviations corresponding to that ill-conditioned submatrix. Consequently, those element deviations will have large errors. Moreover, since one of these values is used to solve for the next couple of element deviations, then this large error will propagate to the remaining parameter calculations. In order to cure such a situatuion, we need to break that ill-conditioned submatrix and reorder the elements such that the corresponding elements are placed at the bottom.

As an example illustrating how such scheme is done, consider the ladder network in Figure 3.5, where the submatrix corresponding to elements Y_{2k-1} and Y_{2k} is ill-conditioned. In this case, we will choose a different set of adjoint circuits. The ith adjoint circuit will be the same as the original circuit except node i is excited by a 1A current source, and both nodes i-1 and i+1 are shorted (except when i=1, only node 2 is shorted, and when i=n+1, only node n is shorted). We do this for i=1,2,....,k-1,n+1,n,n-1,....,k+1,k , in this order. Then, in Eq. (3.22), the previously ill-conditioned submatrix will no longer exist.

Another important practical aspect is the choice of test frequency(s). This is discussed in detail in [5]. It was noticed that the test frequency(s) in the neighborhood of the poles and zeros of the circuit's transfer functions yielded the most information. Furthermore, it is obvious that choosing a frequency(s) that is(are) deep in the stop band of the circuit is a bad choice. It is also recommended that if more than one frequency is to be chosen, then, they should not be adjacent in a flat band, but, they should be chosen in different slope segments of the output frequency response,i.e., they should interlace

with the circuit's poles. Sometimes, changing the test frequency(s) may be used to cure an ill-conditioned submatrix situation.

CHAPTER 4

INSUFFICIENT TEST DATA

4.1 INTRODUCTION

It was shown in the previous chapter that if all the node voltages are accessible, then in the case of linear circuits, there is a linear relation between the circuit parameter changes and certain voltage changes. Furthermore, one can generate an appropriate number of tests such that the system of equations has a rank equal to the number of unknown parameters. In practice, it may not be feasible to measure all node voltages, i.e. a subgroup of nodes in a circuit may be accessible, while the rest of nodes may not. By an accessible node, we mean that we can measure its voltage, and we can apply any type of excitation to it (either current or voltage source). Consequently, we expect to have less test data than we need to solve for the circuit parameter deviations, that is, the number of unknown parameters will exceed the number of equations when only a single test frequency is assumed.

4.2 FAULT IDENTIFICATION UNDER INSUFFICIENT TEST DATA

Consider the linear circuit N in Figure 4.1, which has b parameters, and m accessible ports, where $m<b$. Assume that the circuit N is excited at port 1 with a current source, and the voltages of all the accessible m-ports are measured at the same frequency. Consider, also, the adjoint circuit $\hat{N}$ of the circuit N, Figure 4.2. Assume that

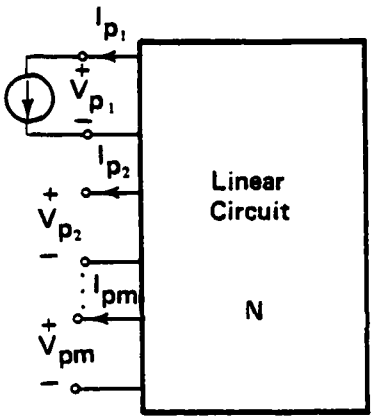


Fig. 4.1 Linear circuit with m accessible ports.

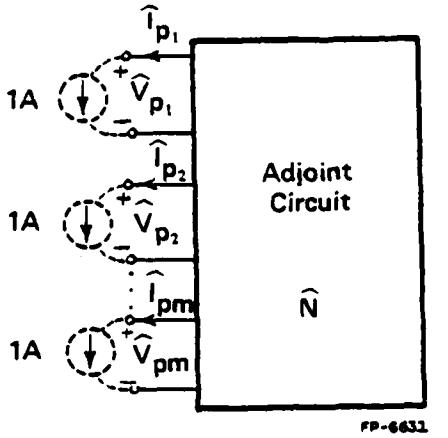


Fig. 4.2 Adjoint circuit of circuit under test.

we excite the adjoint circuit at the jth port by a 1A current source. Then Eq. (3.14) becomes

$$\sum_{k=1}^{b} (X_k + \Delta X_k)\, \hat{X}_k\, \Delta P_k = \Delta V_{pj} \qquad \ldots.(4.1)$$

which could be rewritten as

$$\sum_{k=1}^{b} S_{P_k}^{V_{pj}} \left(1+\frac{\Delta X_k}{X_k}\right) \frac{\Delta P_k}{P_k} = \frac{\Delta V_{pj}}{V_{pj}} \qquad \ldots.(4.2)$$

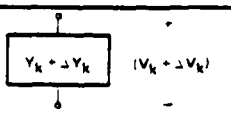
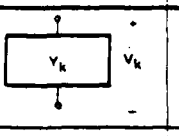
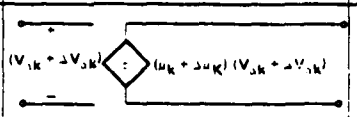
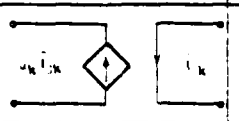
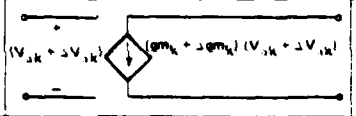
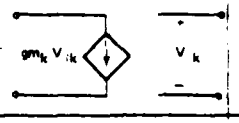
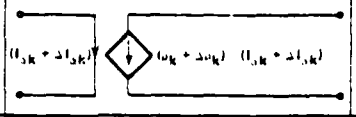
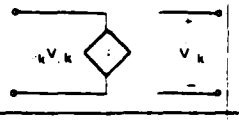
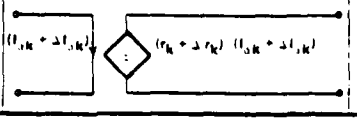
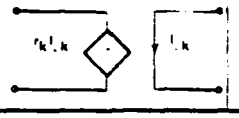
where P_k and X_k are as given in table II, and $S_{P_k}^{V_{pj}}$ is the first-order normalized sensitivity of port voltage V_{pj} with respect to parameter P_k and is given by [15]

$$S_{P_k}^{V_{pj}} = \frac{\partial V_{pj}}{\partial P_k} \frac{P_k}{V_{pj}} \qquad \ldots.(4.3)$$

Table II also gives expressions for the first-order sensitivities for different circuit elements and the circuit constraints for both test and adjoint circuits.

Since we assume that we have access to only a subgroup of the circuit nodes, then this means that we cannot measure all branch voltages, i.e., some of the X_k's in Eq. (4.2) will be unknown. In this case, we have to include the quantities $(1 + \frac{\Delta X_k}{X_k})$ with the unknown vector, i.e.,we consider that the unknowns are the $(1 + \frac{\Delta X_k}{X_k}) \frac{\Delta P_k}{P_k}$'s. By doing so, we restrict our measurements to one and only one test condition, i.e., the same excitation at the same frequency.

TABLE II THE CIRCUIT CONSTRAINTS AND THE SENSITIVITY EXPRESSIONS FOR THE DIFFERENT CIRCUIT ELEMENTS.

Element	P_k	X_k	Circuit Constraints		$S_{P_k}^{V_{pj}}$
			Test Circuit	Adjoint Circuit	
Admittance G,C, Γ	Y_k	V_k			$V_k I_{ak} \frac{Y_k}{V_{pj}}$
VCVS	μ_k	V_{ak}			$-V_{ak} I_{ak} \frac{\mu_k}{V_{pj}}$
VCCS	gm_k	V_{ak}			$V_{ak} V_{ak} \frac{gm_k}{V_{pj}}$
CCCS	α_k	I_{ak}			$I_{ak} V_{ak} \frac{\alpha_k}{V_{pj}}$
CCVS	r_k	I_{ak}			$-I_{ak} I_k \frac{r_k}{V_{pj}}$

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Then, we can obtain only m linear independent equations, if we let j=1,2,.....,m in Eq. (4.2). They have the following form

$$\begin{bmatrix} S_{P_1}^{V_{p1}} & S_{P_2}^{V_{p1}} & \cdots & S_{P_b}^{V_{p1}} \\ S_{P_1}^{V_{p2}} & S_{P_2}^{V_{p2}} & \cdots & S_{P_b}^{V_{p2}} \\ \vdots & \vdots & & \vdots \\ S_{P_1}^{V_{pm}} & S_{P_2}^{V_{pm}} & \cdots & S_{P_b}^{V_{pm}} \end{bmatrix} \begin{bmatrix} (1+\frac{\Delta X_1}{X_1})\frac{\Delta P_1}{P_1} \\ (1+\frac{\Delta X_2}{X_2})\frac{\Delta P_2}{P_2} \\ \vdots \\ (1+\frac{\Delta X_b}{X_b})\frac{\Delta P_b}{P_b} \end{bmatrix} = \begin{bmatrix} \frac{\Delta V_{p1}}{V_{p1}} \\ \frac{\Delta V_{p2}}{V_{p2}} \\ \vdots \\ \frac{\Delta V_{pm}}{V_{pm}} \end{bmatrix} \quad \ldots.(4.4)$$

Eq. (4.4) in an under estimated system, which means that there are infinite number of solutions to it. In order to overcome this difficulty , we will assume that we have only m-1 or less faulty elements. This assumption is reasonable from the practical point of view, since usually only a few elements in a circuit become faulty. This means that the unknowns corresponding to the faulty elements will be nonzero , while those corresponding to the nonfaulty elements will be zero. Hence, the problem will reduce to the following. Given m linear equations in b unknowns (b>m), where m-1 or less of those unknowns are nonzero, while the rest of them are zero. We need to point out the nonzero unknowns corresponding to the faulty elements.

This problem could be solved by considering a subgroup of m elements in Eq. (4.4), and solving for them. Then, by doing so for all different combinations of m elements, the faulty elements may be recognized as the group of m-1 (or less) elements which has a consistent solution among the obtained solutions.

Another alternative and computationally more efficient way is by deleting a subgroup of m-1 unknowns in Eq. (4.4), so that we obtain

just one equation in the rest of the b-m+1 unknowns. Then, if the right-hand side of this equation is zero, the deleted unknowns may correspond to the group of faulty elements. Note that, having a consistent solution in the first way is only a necessary condition, but it is not sufficient. This means that , in some situations, we may have more than one group of m-1 elements satisfying that necessary condition. Such situations depend upon the structure of the circuit and the location of the faulty elements with respect to the location of the accessible test nodes.

The following is an example to show that this approach may detect multiple faults, i.e., either detect the faulty elements or isolate them in a part of the circuit.

Example

Consider the resistive ladder circuit in Figure 4.3, where we have access only to three nodes, as well as to the reference node (m=3). Then,we can have only three equations under the same test condition, and we can only detect or isolate up to two faults. The three equations will be

$$\begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array}\begin{array}{c} \begin{array}{ccccccccccccc} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 \end{array} \\ \begin{bmatrix} X & X & X & X & X & X & X & X & X & X & X & X & X \\ X & X & X & X & X & X & X & X & X & X & X & X & X \\ X & X & X & X & X & X & X & X & X & X & X & X & X \end{bmatrix} \end{array} \underline{u} = \begin{bmatrix} (\Delta V_{p1}/V_{p1}) \\ (\Delta V_{p2}/V_{p2}) \\ (\Delta V_{p3}/V_{p3}) \end{bmatrix} \qquad \ldots.(4.5)$$

where an X in the ijth position will be $S_{G_j}^{V_{pi}}$, and $\underline{u}$ corresponds to the unknown vector of dimension 13.

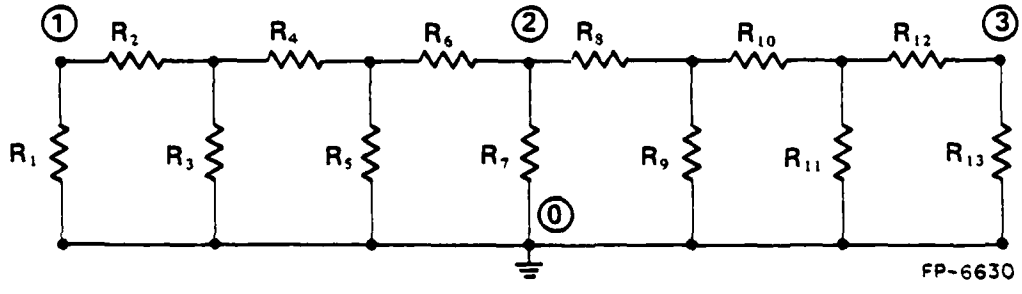

Fig. 4.3 Example of a resistive ladder circuit with only three accessible ports.

Since the three adjoint circuits are excited by a 1A current source at nodes 1,2 and 3, respectively. Then, we can see that the two portions of Eq. (4.5) boxed by a solid line are dependent, and the same thing applies to those with the dashed line. This means that, if we have a double fault , such that one of the faulty elements is in the group $\{R_1,R_2,.....,R_7\}$, and the other is in $\{R_7,R_8,.....,R_{13}\}$, then, the faulty elements can be identified uniquely using the above deletion of variables scheme. However, if we have a double fault, such that the two faulty elements are in the group $\{R_1,R_2,.....,R_7\}$ (or $\{R_7,R_8,.....,R_{13}\}$), then any two elements of this group will appear faulty using the same scheme. This means that, in this case, we can only isolate the double fault in a part of the circuit. In order to narrow down the group of possibly faulty elements, more accessible nodes in this part of the circuit are needed.

In the next section , we explain this method for the case in which only a single fault is assumed and only two nodes plus a reference node are accessible.

4.3 SINGLE FAULT IDENTIFICATION

The single fault identification problem is a common problem. In this case, it is assumed that one and only one fault occurs in a circuit. This is sometimes the most likely situation in practice. Using our approach, it is enough to have access to only two nodes in the circuit (input and output nodes, say) as well as a reference node in order to identify a single fault. An algorithm for single fault identification will be presented in the next section. Another modified algorithm will be presented later to handle the problem of single fault

identification if the nonfaulty elements are within a prescribed tolerance from their nominal values.

4.3.1 SINGLE FAULT AMONG ZERO-TOLERANCED ELEMENTS

Here, we assume that we have only a single fault, while the rest of elements assume their nominal values. Since we assume that we have only two accessible ports in the test circuit (m=2), then we have only two linear equations in b unknowns. In addition, we know that one and only one unknown is nonzero, while the rest of the b-1 unknowns are zero. Assume that the faulty element is P_l , where $1 \leq l \leq b$. Then, Eq. (4.4) will reduce to

$$S_{P_l}^{V_{p1}} \left(1 + \frac{\Delta X_l}{X_l}\right) \frac{\Delta P_l}{P_l} = \frac{\Delta V_{p1}}{V_{p1}} \qquad ..(4.6\text{-a})$$

and

$$S_{P_l}^{V_{p2}} \left(1 + \frac{\Delta X_l}{X_l}\right) \frac{\Delta P_l}{P_l} = \frac{\Delta V_{p2}}{V_{p2}} \qquad ..(4.6\text{-b})$$

The solution of Eq. (4.6-a) must be consistent with that of Eq. (4.6-b). Hence, for the faulty element, we must have the following relationship

$$\frac{(\Delta V_{p1}/V_{p1})}{S_{P_l}^{V_{p1}}} = \frac{(\Delta V_{p2}/V_{p2})}{S_{P_l}^{V_{p2}}} \qquad ....(4.7)$$

This relationship could be used to determine the value of l, i.e., to identify the faulty element. A further step after the identification of

the faulty element would be the calculation of the value of the faulty component. This would be very straightforward if we could measure the corresponding ΔX_1. However, this may not be possible, since we have access to only two ports of the circuit. Hence, we will have to look for an alternative way.

An expression for ΔX_1 could be obtained through the bilinear transformation. Since any response in a circuit can be written in terms of one parameter in the bilinear form [6], then X_1 could be expressed in terms of P_1 as

$$X_1 = \frac{A P_1 + B}{C P_1 + D} \qquad ....(4.8)$$

where A,B,C and D are constants that do not depend on P_1, with the property that

$$A D - B C \neq 0 \qquad ....(4.9)$$

Moreover, since X_1 is the controlling voltage or current for element P_1 (Table I), then it can be easily shown that always A=0 , for any circuit element. Then Eq. (4.9) reduces to

$$X_1 = \frac{B}{C P_1 + D} \qquad ...(4.10)$$

Now, assume that only the parameter P_1 changes to $P_1 + \Delta P_1$, consequently $X_1 \longrightarrow X_1 + \Delta X_1$, which will be given by

$$X_1 + \Delta X_1 = \frac{B}{C(P_1 + \Delta P_1) + D} \qquad \ldots(4.11)$$

By dividing Eq. (4.11) by Eq. (4.10), we get

$$1 + \frac{\Delta X_1}{X_1} = \frac{1}{1 + \alpha_1 (\frac{\Delta P_1}{P_1})} \qquad \ldots(4.12)$$

where

$$\alpha_1 = \frac{CP_1}{CP_1 + D} \qquad \ldots(4.13)$$

From Eqs. (4.6),(4.7) and (4.12), we have

$$\frac{\Delta P_1}{P_1} = (\frac{\Delta V_{pj}}{V_{pj}}) / [S_{P_1}^{V_{pj}} - \alpha_1 (\frac{\Delta V_{pj}}{V_{pj}})] \quad ;j=1,2 \qquad \ldots(4.14)$$

which is an expression for the relative error in the parameter P_1. The constant α_1 could be calculated in two ways. The first way, is by rewriting Eq. (4.13) as

$$\alpha_1 = 1 - \frac{D}{CP_1+D} = 1 - \frac{\frac{B}{CP_1+D}}{\frac{B}{D}} = 1 - \frac{X_1|_{\text{nominal}}}{X_1|_{P_1=0}} \qquad \ldots(4.15)$$

which needs, in addition, an analysis for the circuit with nominal values except the parameter P_1 is set to zero.

The other way would be by partially differentiating X_1 (in Eq.

(4.10))with respect to P_1

$$\frac{\partial X_1}{\partial P_1} = \frac{-BC}{(CP_1+D)^2} \qquad \ldots(4.16)$$

Then, we use Eq. (4.3) to get an expression for the first-order sensitivity of X_1 with respect to P_1.

$$S_{P_1}^{X_1} = \frac{\partial X_1}{\partial P_1}\frac{P_1}{X_1} = \frac{-C\,P_1}{CP_1+D} \qquad \ldots(4.17)$$

From Eqs. (4.13) and (4.17), we see that

$$\alpha_1 = -S_{P_1}^{X_1} \qquad \ldots(4.18)$$

which also needs, in addition, an analysis of the adjoint circuit with a 1A current source connected across X_1 as an excitation. However, this way is more computationally efficient than the first way , because the second way does not need another LU decomposition, while the first way does.

Based on the previous results, the algorithm for single fault identification will be as follows.

<u>The algorithm:</u>

(1) Calculate the first-order sensitivities $S_{P_k}^{V_{p1}}$ and $S_{P_k}^{V_{p2}}$; k=1,2,.....,b.

(2) Measure the quantities ΔV_{p1} and ΔV_{p2} under the same test condition.

(3) Calculate the quantities $C_k^{(1)} = (\frac{\Delta V_{p1}}{V_{p1}})/S_{P_k}^{V_{p1}}$ and

$$C_k^{(2)} = \left(\frac{\Delta V_{p2}}{V_{p2}}\right)/S_{P_k}^{V_{p2}} \quad ; \quad k=1,2,.....,b.$$

(4)(a) If $|C_k^{(1)}-C_k^{(2)}|=0$;for all k=1,2,.....,b, this means that there is no fault.

(b) If $|C_{l_i}^{(1)}-C_{l_i}^{(2)}|=0$;for some i=1,2,....,p , where $1\leq l_1,l_2,....,l_p\leq b$, and where $P_{l_1},P_{l_2},.....,P_{l_p}$ are parallel elements, and $|C_k^{(1)}-C_k^{(2)}|\neq 0$;for k=1,2,.....,b and $k\neq l_1,l_2,....,l_p$, this means that one or more of the parallel group $P_{l_1},P_{l_2},.....,P_{l_p}$ are faulty.

(c) Otherwise, there is more than one fault.

(5) Calculate α_1 by either of the following ways

(a) Solve the original circuit with nominal parameters except that $P_1=0$ and use Eq. (4.15), or,

(b) solve the adjoint circuit with a 1A current source across X_1 as an excitation, and calculate the first-order sensitivity of X_1 with respect to P_1, i.e., $S_{P_1}^{X_1}$, then, use Eq. (4.18).

(6) Calculate the relative error in the faulty parameter P_1 using Eq. (4.14) for either j=1 or 2.

Computationally, the algorithm needs the analysis of one original and three adjoint circuits for the identification and calculation of a single fault. However, since the nodal matrix for the adjoint network is the transpose of that for the original network, then, we need to perform the matrix inversion or LU decomposition only once. The rest of calculations will be straightforward . This indicates that the algorithm is highly computationally efficient with no required storage and with minimum measurements, on the contrary to the fault dictionary approach.

In the next section, we will modify the same algorithm to detect single faults when the rest of parameters are within a prescribed tolerance from their nominal values.

4.3.2 SINGLE FAULT AMONG NONZERO-TOLERANCED ELEMENTS

Here, we will require less stringent assumptions on the faulty network. Specifically, we assume that we have only a single fault, while the other element values are within a specified tolerance (say δ) from their nominal values. Of course, we require that the relative error in the faulty parameter be clearly distinguishable from the relative error in the good parameters. This situation is much more practical than the case discussed in the previous section. This is because a manufactured circuit will not have component values equal to the nominal design values, but only within some specified tolerance of their nominal values. In the following, we will see how we may identify the faulty parameter under the above assumptions.

Assume that the faulty parameter is P_l, where $1 \leq l \leq b$. Assume also that all the other parameters are within some tolerance of their nominal values, for example

$$\left|\frac{\Delta P_k}{P_k}\right| \leq \delta \qquad \text{;for all } k=1,2,\ldots,b \text{ and } k \neq l \qquad \ldots(4.19)$$

and where δ is the maximum allowed relative tolerance, $\delta \geq 0$.

Next, we will calculate the change in the response X_k of the parameter P_k due to the change in all the parameters. We will assume that first-order sensitivity values can be used to obtain a reasonable estimate of the effect of the deviation of the good parameters from

their nominal values. Thus, we write

$$\Delta X_k \equiv \sum_{\substack{i=1 \\ i\neq 1}}^{b} \frac{\partial X_k}{\partial P_i} \Delta P_i + \Delta X_{k1} \qquad \ldots(4.20)$$

where ΔX_{k1} is the change in X_k due to only a change in P_1. By dividing both sides of Eq. (4.20) by X_k, then adding 1 to both sides, we get

$$1 + \frac{\Delta X_k}{X_k} \equiv (1 + \frac{\Delta X_{k1}}{X_k}) + \sum_{\substack{i=1 \\ i\neq 1}}^{b} S_{P_i}^{X_k} (\frac{\Delta P_i}{P_i}) \qquad \ldots(4.21)$$

where $S_{P_i}^{X_k}$ is the first-order sensitivity of X_k with respect to P_i, given by Eq. (4.3).

As stated in the previous section, that we can express X_k as a function of P_1 in the bilinear form as follows

$$X_k = \frac{A_k P_1 + B_k}{C_k P_1 + D_k} \quad ;k=1,2,.....,b \qquad \ldots(4.22)$$

Note that $A_1=0$. When only $P_1 \longrightarrow P_1 + \Delta P_1$, then $X_k \longrightarrow X_k + \Delta X_{k1}$, and we have

$$X_k + \Delta X_{k1} = \frac{A_k(P_1 + \Delta P_1) + B_k}{C_k(P_1 + \Delta P_1) + D_k} \quad ;k=1,2,.....,b \qquad \ldots(4.23)$$

Dividing Eq. (4.23) by (4.22), we get

$$1 + \frac{\Delta X_{k1}}{X_k} = \frac{1 + \beta_k(\Delta P_1/P_1)}{1 + \alpha_k(\Delta P_1/P_1)} \quad ;k=1,2,.....,b \qquad \ldots(4.24)$$

where

$$\alpha_k = \frac{C_k P_1}{C_k P_1 + D_k} \quad \text{,and} \quad \beta_k = \frac{A_k P_1}{A_k P_1 + B_k} \qquad \ldots(4.25)$$

Now, we will try to get a relationship between α_k and β_k. By partially differentiating X_k with respect to P_1 in Eq. (4.22), we get

$$\frac{\partial X_k}{\partial P_1} = \frac{A_k D_K - B_k C_k}{(C_k P_1 + D_k)^2} \qquad \ldots(4.26)$$

From Eqs. (4.3),(4.22),(4.25) and (4.26), we get the relationship

$$\beta_k = \alpha_k + S_{P_1}^{X_k} \qquad \ldots(4.27)$$

Note that $\beta_1 = 0$, which gives Eq. (4.18). Substituting from Eq. (4.27) into Eq. (4.24), we get

$$1 + \frac{\Delta X_{kl}}{X_k} = 1 + \frac{S_{P_1}^{X_k}(\Delta P_1/P_1)}{1 + \alpha_k(\Delta P_1/P_1)} \qquad \ldots(4.28)$$

Again, substituting from Eq. (4.28) into Eq. (4.24), and then, into Eq. (4.2), we get

$$\sum_{k=1}^{b} S_{P_k}^{V_{pj}} \left[1 + \frac{S_{P_1}^{X_k}(\Delta P_1/P_1)}{1+\alpha_k(\Delta P_1/P_1)} \right] \rightarrow \sum_{\substack{i=1 \\ i \neq 1}}^{b} S_{P_i}^{X_k}(\Delta P_i/P_i)](\frac{\Delta P_k}{P_k}) \equiv \frac{\Delta V_{pj}}{V_{pj}} \quad ;j=1,2 \qquad \ldots(4.29)$$

Eq. (4.29) can be rewritten as (using $\alpha_1 = -S_{P_1}^{X_1}$)

$$\left(\frac{\Delta P_1}{P_1}\right)\left[\frac{1}{1+\alpha_1(\Delta P_1/P_1)}+\sum_{\substack{i=1\\ i\neq 1}}^{b} S_{P_i}^{X_1}\left(\frac{\Delta P_i}{P_i}\right)\right]\equiv\frac{(\Delta V_{pj}/V_{pj})}{S_{P_1}^{V_{pj}}}$$

$$-\frac{1}{S_{P_1}^{V_{pj}}}\sum_{\substack{k=1\\ k\neq 1}}^{b} S_{P_k}^{V_{pj}}\left(\frac{\Delta P_k}{P_k}\right)\left[1+\frac{S_{P_1}^{X_k}(\Delta P_1/P_1)}{1+\alpha_k(\Delta P_1/P_1)}+\sum_{\substack{i=1\\ i\neq 1}}^{b} S_{P_i}^{X_k}\left(\frac{\Delta P_i}{P_i}\right)\right]\ ;j=1,2 \qquad \ldots(4.30)$$

Next, we will simplify Eq. (4.30) using the assumption that the absolute relative error in the faulty parameter $\left|\frac{\Delta P_1}{P_1}\right|$ is distinguishably greater than the maximum tolerance value . Specifically, we will study two cases. In the first case, we will consider a positive fault, i.e., the faulty parameter has a value above its nominal value. In the second case, we will consider a negative fault, i.e., the faulty parameter has a value below its nominal value.

Case I

Here, we assume that the faulty parameter has a value greater than its nominal value, i.e., $0<\frac{\Delta P_1}{P_1}<\infty$. Moreover, we assume that $\left|\frac{\Delta P_1}{P_1}\right|$ is high enough, such that

$$\left|\alpha_k\left(\frac{\Delta P_1}{P_1}\right)\right| >> 1 \quad \text{;at least for } k=1,2,\ldots,b \text{ and } k\neq 1 \qquad \ldots(4.31)$$

Using this assumption Eq. (4.30) reduces to

$$\left(\frac{\Delta P_1}{P_1}\right)\left[\frac{1}{1+\alpha_1(\Delta P_1/P_1)} + \sum_{\substack{i=1\\ i\neq 1}}^{b} S_{P_i}^{X_1}\left(\frac{\Delta P_i}{P_i}\right)\right] \equiv \frac{(\Delta V_{pj}/V_{pj})}{S_{P_1}^{V_{pj}}}$$

$$- \frac{1}{S_{P_1}^{V_{pj}}} \sum_{\substack{k=1\\ k\neq 1}}^{b} S_{P_k}^{V_{pj}}\left(\frac{\Delta P_k}{P_k}\right)\left[1+\frac{S_{P_1}^{X_k}}{\alpha_k} + \sum_{\substack{i=1\\ i\neq 1}}^{b} S_{P_i}^{X_k}\left(\frac{\Delta P_i}{P_i}\right)\right] \quad ;j=1,2 \qquad \ldots(4.32)$$

Consider the term

$$1+\frac{S_{P_1}^{X_k}}{\alpha_k} = \frac{\alpha_k + S_{P_1}^{X_k}}{\alpha_k} = \frac{\beta_k}{\alpha_k} = \frac{X_k|_{P_1=\infty}}{X_k|_{\text{nominal}}} \qquad \ldots(4.33)$$

In deriving Eq. (4.33), we used Eqs. (4.22),(4.25) and (4.27). Substituting from Eq. (4.33) into Eq. (4.32), we get

$$Q_1^{(j)} \equiv C_1^{(j)} - d_1^{(j)} \quad ;j=1,2 \qquad \ldots(4.34)$$

where

$$Q_1^{(j)} = \left(\frac{\Delta P_1}{P_1}\right)\left[\frac{1}{1+\alpha_1(\Delta P_1/P_1)} + \sum_{\substack{i=1\\ i\neq 1}}^{b} S_{P_i}^{X_1}\left(\frac{\Delta P_i}{P_i}\right)\right] \qquad \ldots(4.35)$$

and

$$C_1^{(j)} = \frac{(\Delta V_{pj}/V_{pj})}{S_{P_1}^{V_{pj}}} \qquad \ldots(4.36)$$

and

$$d_1^{(j)} = \frac{1}{S_{P_1}^{V_{pj}}} \sum_{\substack{k=1 \\ k\neq 1}}^{b} S_{P_k}^{V_{pj}} \left(\frac{\Delta P_k}{P_k}\right) \left[\frac{X_k|_{P_1=\infty}}{X_k|_{\text{nominal}}} + \sum_{\substack{i=1 \\ i\neq 1}}^{b} S_{P_i}^{X_k} \left(\frac{\Delta P_i}{P_i}\right)\right] \qquad \ldots(4.37)$$

Let

$$D_1^{(j)} = \max |d_1^{(j)}|$$

$$= \frac{1}{\left|S_{P_1}^{V_{pj}}\right|} \sum_{\substack{k=1 \\ k\neq 1}}^{b} \delta \left|S_{P_k}^{V_{pj}}\right| \left[\left|\frac{X_k|_{P_1=\infty}}{X_k|_{\text{nominal}}}\right| + \delta \sum_{\substack{i=1 \\ i\neq 1}}^{b} \left|S_{P_i}^{X_k}\right|\right] \qquad \ldots(4.38)$$

Case II

Now, we assume that the faulty parameter has a value less than its nominal value, i.e., $-1 \leq \frac{\Delta P_1}{P_1} < 0$. In addition, we assume that $\left|\frac{\Delta P_1}{P_1}\right|$ is high enough, such that

$$\frac{\Delta P_1}{P_1} \cong -1 \qquad \ldots(4.39)$$

Hence, Eq. (4.30) reduces to

$$\left(\frac{\Delta P_1}{P_1}\right)\left[\frac{1}{1+\alpha_1(\Delta P_1/P_1)} + \sum_{\substack{i=1 \\ i\neq 1}}^{b} S_{P_i}^{X_1} \left(\frac{\Delta P_i}{P_i}\right)\right] \cong \frac{(\Delta V_{pj}/V_{pj})}{S_{P_1}^{V_{pj}}}$$

$$- \frac{1}{S_{P_1}^{V_{pj}}} \sum_{\substack{k=1 \\ k\neq 1}}^{b} S_{P_k}^{V_{pj}} \left(\frac{\Delta P_k}{P_k}\right) \left[1 - \frac{S_{P_1}^{X_k}}{1-\alpha_k} + \sum_{\substack{i=1 \\ i\neq 1}}^{b} S_{P_i}^{X_k} \left(\frac{\Delta P_i}{P_i}\right)\right] \quad ; j=1,2 \qquad \ldots(4.40)$$

Consider the term

$$1-\frac{S_{P_1}^{X_k}}{1-\alpha_k}=\frac{1-(\alpha_k+S_{P_1}^{X_k})}{1-\alpha_k}=\frac{1-\beta_k}{1-\alpha_k}=\frac{X_k|_{P_1=0}}{X_k|_{nominal}} \qquad ...(4.41)$$

In deriving Eq. (4.41), we used Eqs. (4.22),(4.25) and (4.27). Substituting from (4.41) into (4.40), we get

$$Q_1^{(j)} \cong C_1^{(j)} - e_1^{(j)} \quad ;j=1,2 \qquad ...(4.42)$$

where $Q_1^{(j)}$ and $C_1^{(j)}$ are as given by Eqs. (4.35) and (4.36), respectively, and

$$e_1^{(j)}=\frac{1}{S_{P_1}^{V_{pj}}}\sum_{\substack{k=1\\k\neq 1}}^{b} S_{p_k}^{V_{pj}}\left(\frac{\Delta P_k}{P_k}\right)\left[\frac{X_k|_{P_1=0}}{X_k|_{nominal}}+\sum_{\substack{i=1\\i\neq 1}}^{b} S_{P_i}^{X_k}\left(\frac{\Delta P_i}{P_i}\right)\right] \qquad ...(4.43)$$

Let

$$E_1^{(j)}=\max|e_1^{(j)}|$$

$$=\frac{1}{\left|S_{P_1}^{V_{pj}}\right|}\sum_{\substack{k=1\\k\neq 1}}^{b}\delta\left|S_{p_k}^{V_{pj}}\right|\left[\left|\frac{X_k|_{P_1=0}}{X_k|_{nominal}}\right|+\delta\sum_{\substack{i=1\\i\neq 1}}^{b}\left|S_{P_i}^{X_k}\right|\right] \qquad ...(4.44)$$

From Eqs. (4.34) and (4.42), it is necessary for the faulty parameter P_1 to have almost equal values of $Q_1^{(j)}$ for j=1 and 2, i.e. , $Q_1^{(1)} \cong Q_1^{(2)}$, under case I or case II. This is because the quantity $Q_1^{(j)}$ does not depend upon the value of j , as seen from Eq. (4.35).

There will be a minor problem when we try to calculate the

quantities $d_1^{(j)}$ and $e_1^{(j)}$ using Eqs. (4.37) and (4.43), respectively. This is because we do not know the actual value of $\frac{\Delta P_i}{P_i}$; i=1,2,.....,b and i≠1 for the good parameters. However, we do know that $|\frac{\Delta P_i}{P_i}| \leq \delta$; i=1,2,.....,b and i≠1. Hence, we can calculate the maximum possible values of both $d_1^{(j)}$ and $e_1^{(j)}$, which are given by Eqs. (4.38) and (4.44). Then, $Q_1^{(j)}$ should be somewhere in the interval $[C_1^{(j)}-D_1^{(j)}, C_1^{(j)}+D_1^{(j)}]$ for case I, and for case II, $Q_1^{(j)}$ should be within the interval $[C_1^{(j)}-E_1^{(j)}, C_1^{(j)}+E_1^{(j)}]$. This implies that we should have an overlapping of the two intervals corresponding to j=1 and 2, for case I or case II. A necessary and sufficient condition for that overlapping requirement is that

$$|C_1^{(1)}-C_1^{(2)}| \leq D_1^{(1)}+D_1^{(2)} \quad \text{;for case I} \qquad \ldots(4.45)$$

and

$$|C_1^{(1)}-C_1^{(2)}| \leq E_1^{(1)}+E_1^{(2)} \quad \text{;for case I} \qquad \ldots(4.46)$$

It is not easy to calculate the exact value of the faulty component, because we do not know the actual value of $\frac{\Delta P_i}{P_i}$; i=1,2,.....,b and i≠1. However, one can have an expected value of it, by taking the expectation of both sides of Eq. (4.34) and Eq. (4.42) for case I and case II, respectively. Or, one can obtain a range where the faulty parameter value will be, by using Eqs. (4.34),(4.35),(4.36) and (4.38) for case I, and Eqs. (4.42),(4.35),(4.36) and (4.44) for case II.

Based on the previous results, an algorithm for single fault

identification among nonzero-toleranced parameters will be as follows:

The Algorithm

(1) Calculate the first-order sensitivities $S_{P_k}^{V_{p1}}$, $S_{P_k}^{V_{p2}}$ and $S_{P_i}^{V_k}$; for all k,i=1,2,.....,b.

(2) Measure the quantities ΔV_{p1} and ΔV_{p2}.

(3) Calculate the quantities $C_k^{(1)}$ and $C_k^{(2)}$; k=1,2,.....,b using Eq. (4.36).

(4) Solve the original circuit with nominal values except $P_k = \infty$ once and again with $P_k = 0$. Do this for k=1,2,.....,b.

(5) Calculate the quantities $D_1^{(1)}, D_1^{(2)}, E_1^{(1)}$ and $E_1^{(2)}$; for all l=1,2,.....,b, using Eqs. (4.38) and (4.44).

(6)(a) If $|C_k^{(1)} - C_k^{(2)}| \leq D_k^{(1)} + D_k^{(2)}$, and $|C_k^{(1)} - C_k^{(2)}| \leq E_k^{(1)} + E_k^{(2)}$; for all k=1,2,.....,b, this means that there is no fault.

(b) If $|C_k^{(1)} - C_k^{(2)}| \leq D_k^{(1)} + D_k^{(1)}$ or $|C_k^{(1)} - C_k^{(2)}| \leq E_k^{(1)} + E_k^{(2)}$; for only $k = l_1, l_2, \ldots, l_p$, where $1 \leq l_1, l_2, \ldots, l_p \leq b$ and $P_{l_1}, P_{l_2}, \ldots, P_{l_p}$ are parallel elements, then this means that one or more of $P_{l_1}, P_{l_2}, \ldots, P_{l_p}$ are faulty.

(c) Otherwise, there is more than one fault, or the algorithm fails because the assumptions made are not met, e.g., a small single fault value relative to the prescribed tolerance value.

We see that in order to add the feature of single fault identification among nonzero-toleranced parameters, we have to pay for extra computations.

In the case where the test circuit is originally excited by a voltage source at the input port, some minor modifications are

necessary. The corresponding first adjoint circuit will be excited at the input port (port 1) by a -1V voltage source, while the second adjoint circuit will be excited by a 1A current source at the output port (port 2) with port 1 short-circuited. In addition, the quantities $S_{P_k}^{V_{p1}}$ and $\frac{\Delta V_{p1}}{V_{p1}}$ will be replaced by $S_{P_k}^{I_{p1}}$ and $\frac{\Delta I_{p1}}{I_{p1}}$, respectively.

If the algorithm fails in a situation, where some parameters of the circuit are within some tolerance of their nominal values, then another run may not fail by switching ports 1 and 2 from the excitation point of view. This will depend upon some factors; a) first-order sensitivity values, b) structure of the circuit, c) location of the single fault with respect to the exciting port, and d) the relative error in the faulty parameter with respect to the specified tolerance.

The method is also capable of identifying catastrophic failures, especially short-circuit faults. For example, if an admittance branch Y_1 becomes short-circuited, then $\frac{\Delta Y_1}{Y_1}=-\infty$, also $1+\frac{\Delta V_1}{V_1}=0$, but the product $(1+\frac{\Delta V_1}{V_1})\frac{\Delta Y_1}{Y_1}$ will have a finite value since $(1+\frac{\Delta V_1}{V_1})\frac{\Delta Y_1}{Y_1} = (\Delta V_{pj}/V_{pj})/S_{Y_1}^{V_{pj}}$; j=1,2, provided that $S_{Y_1}^{V_{pj}} \neq 0$.

Finally, a dc test and an ac test may be able to separate between elements that are in parallel in the ac circuit, but are not in the dc circuit.

4.4 MULTIPLE FAULT DETERMINATION AND ISOLATION SCHEMES

Some other schemes different than the scheme discussed above may be used when some of the nodes in a circuit are inaccessible. As seen before, the technique used in the previous section is most suitable for

single fault identification. Another technique may be used for fault determination and isolation when the number of accessible nodes is more than the number of inaccessible nodes. It also can be used for the fault isolation in a circuit composed of connected subcircuits, e.g., a card of IC chips connected together.

4.4.1 DETERMINATION AND ISOLATION OF FAULTY ELEMENTS IN A CIRCUIT WITH FEW INACCESSIBLE NODES

The following technique will be most useful for circuits with the number of inaccessible nodes fewer than the number of accessible nodes. In such situation, deviation in some elements could be determined exactly, while deviation in the other elements cannot be determined, but we can determine whether or not a fault is present. In fact, the number of elements that could be determined exactly depends upon the number and location of the inaccessible nodes relative to the accessible nodes in a circuit, as well as the structure of the circuit itself. In general, the less the number of inaccessible nodes, the more elements that can be determined exactly.

Consider a circuit N with b branches, and let the set of nodes $\{n_1,n_2,.....,n_l\}$ be the set of accessible nodes each of which is a one terminal of a branch whose other terminal is an inaccessible node. Then, we can split the circuit N into two subcircuits N_1 and N_2,Figure 4.4, such that N_1 contains all the inaccessible nodes together with the elements connected to those inaccessible nodes and every element connected directly between any two nodes of the set $\{n_1,n_2,.....,n_l\}$. While the subcircuit N_2 contains the rest of the accessible nodes together with the rest of branches.

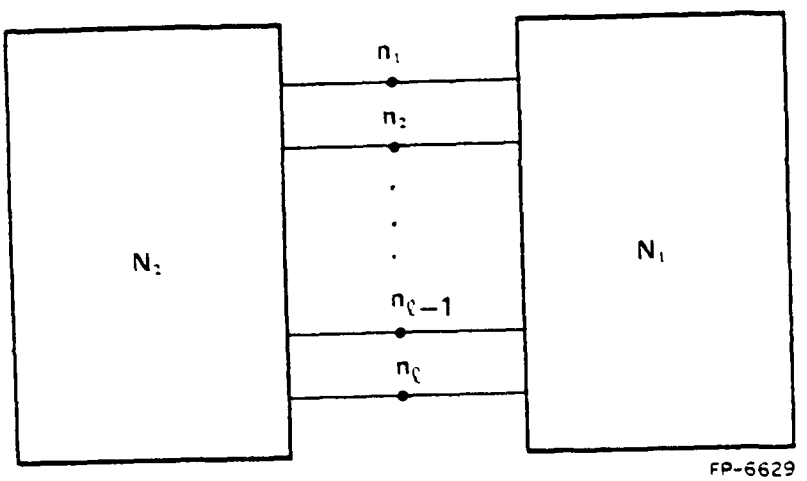

Fig. 4.4 The circuit N is divided into two subcircuits N_1 and N_2.

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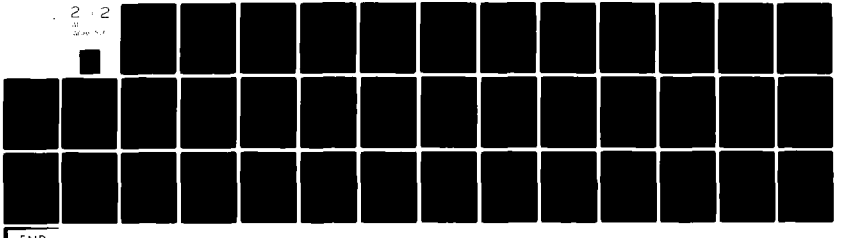

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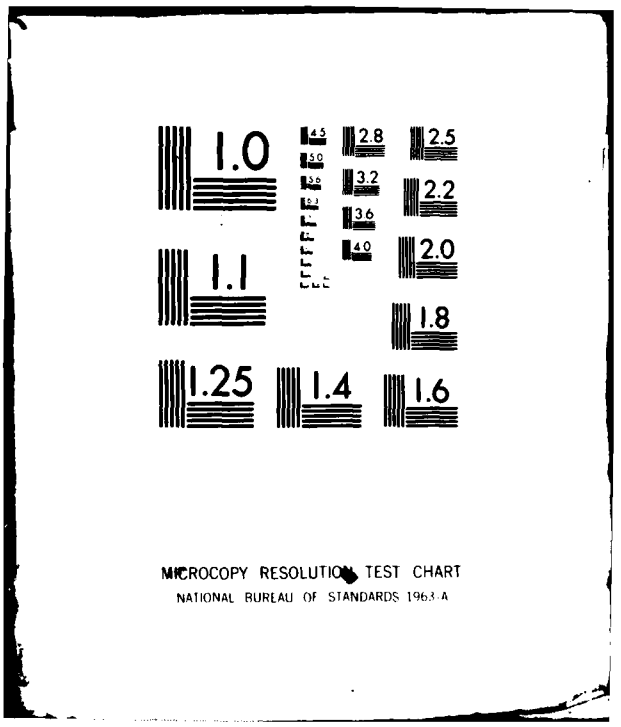
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MICROCOPY RESOLUTION TEST CHART
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Next, we will show how we can determine exactly the element deviations in the subcircuit N_2, and decide whether the subcircuit N_1 has one or more faults, or not. This could be achieved through the choice of the different adjoint circuits. Specifically, by appropriate short-circuits and exciting appropriate nodes with equal voltage sources such that the voltages across all the elements in subcircuit N_1 are zero. Then, the test data and these different adjoint circuits could be used to generate a number of linear equations equal to the number of elements in subcircuit N_2. Solving these equations will yield the deviation in the elements of N_2. Another adjoint circuit or more can be used along with a set of measurements to generate other equations. From the obtained solution for element deviations in N_2 and these last equations, we can decide whether the subcircuit N_1 has one or more faults or not. This technique will be demonstrated through the following example.

Example

Consider the simple circuit shown in Figure 4.5, where only node 6 is assumed to be inaccessible. The circuit is split into two subcircuits, N_1 and N_2, indicated by the dashed line in Figure 4.5.In this example, the set of nodes $\{n_1,n_2,.....,n_l\}$ is $\{4,5\}$. The different adjoint circuits are as shown in Figure 4.6. It is clear from Figure 4.6, that the first four adjoint circuits are chosen such that the voltage across the elements of subcircuit N_1 (elements R_{10},R_{11} and R_{12}) remain zero. By associating these five adjoint circuits with three sets of different measurements (e.g. by exciting the test circuit at nodes 1,2 and 3, then, measuring the accessible node voltages) we obtain the

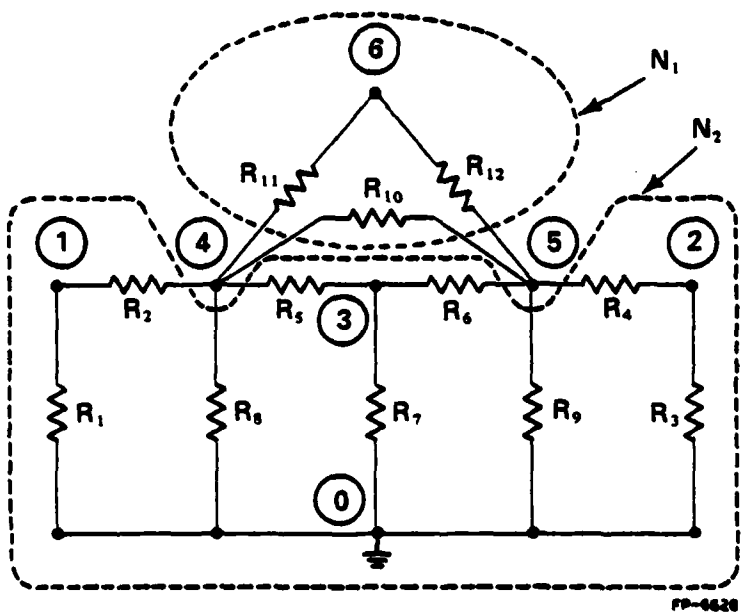


Fig. 4.5 Example of a circuit with one inaccessible node.

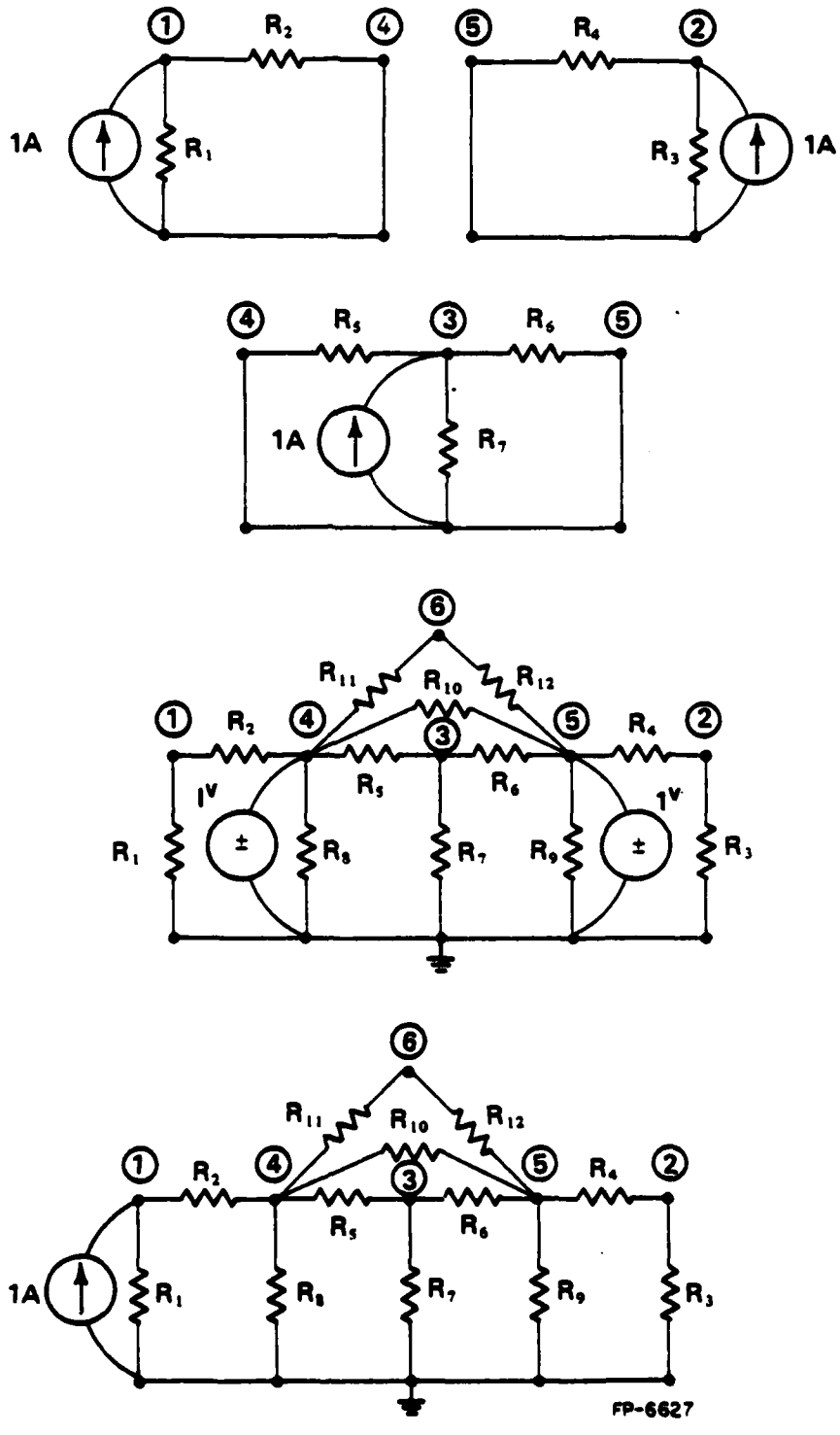
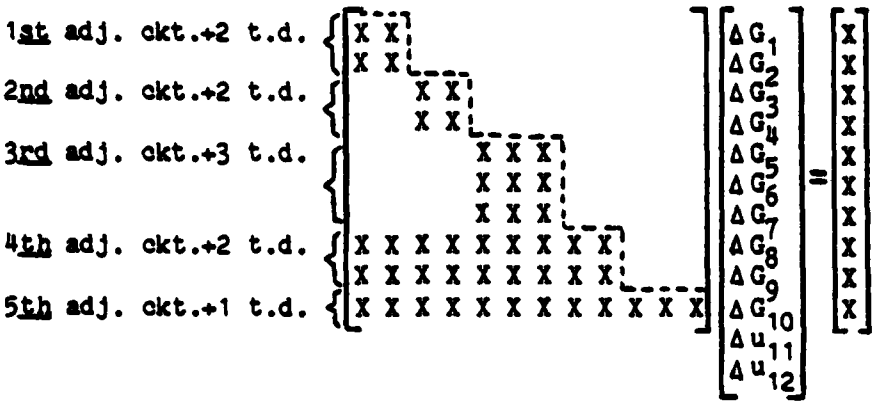


Fig. 4.6 Five adjoint circuits for the circuit of the example.

following system of linear equations.



...(4.47)

where $\Delta u_i=(V_i+\Delta V_i)\Delta G_i$, for i=11 and 12, and an X means a nonzero entry, and a blank means a zero entry. Solving the first nine equations of Eq. (4.47) yields $\Delta G_1,\Delta G_2,.....,\Delta G_9$. Then, by substituting $\Delta G_1,\Delta G_2,.....,\Delta G_9$ in the last equation in Eq. (4.47), we check whether G_{10},G_{11} and G_{12} may be faulty or not (provided that the linear combination we have in the last equation for $\Delta G_{10},\Delta u_{11}$ and Δu_{12} will not result in zero right-hand side value). Note that for this example, we can generate two more equations in $\Delta G_{10},\Delta u_{11}$ and Δu_{12} using two other adjoint circuits (by exciting ports 2 and 3 each at a time by a 1A current source). Then, we can solve the last three equations to determine the values of $\Delta G_{10},\Delta u_{11}$ and Δu_{12} under the corresponding test condition. This will determine ΔG_{10} and whether G_{11} and/or G_{12} are faulty or not.

4.4.2 FAULT ISOLATION IN CIRCUITS COMPOSED OF CONNECTED SUBCIRCUIT BLOCKS

The same scheme can be used for the fault isolation at the block level, i.e.,decide whether a block in a circuit is faulty or not. This

is mainly based on the idea that a block with few accessible nodes could be collapsed by means of an equivalent transformation to a circuit with all accessible nodes. However, we do not actually have to perform that equivalent transformation. To illustrate this technique, we consider the following example.

Example

Consider two single-input single-output subcircuits N_1 and N_2 connected in tandem as shown in Figure 4.7. For simplicity, assume that N_1 and N_2 are linear passive networks. Assume that the input node (node 1), the junction node (node 3), and the output node (node 4) are accessible. Also, assume that, in subcircuit N_1, there is only one impedance (Z_4) connected to the junction node 3, with the other end node 2 being accessible, as well. Then, by means of equivalent transformation, we can model subcircuit N_1 ,excluding Z_4, by an equivalent Π-network, and subcircuit N_2 by an equivalent Π-network, Figure 4.8. By applying the same approach done in the third chapter, we can determine the faults in the equivalent impedances $Z_1, Z_2, \ldots, Z_7$. Then, if we have faults in one or more of $\{Z_1, Z_2, Z_3, Z_4\}$, this implies that the subcircuit N_1 is faulty. Similarly, if we have faults in one or more of $\{Z_5, Z_6, Z_7\}$, this implies that the subcircuit N_2 is faulty.

The assumption that we should have node 2 accessible is important. This is because, if we do not have this node accessible, this means that the impedances Z_3 and Z_5 will be in parallel, which could not be separated under single frequency or dc measurements. Alternatively, we could assume the same assumption for the subcircuit N_2 instead of N_1. In general, we need to assume that, in one of the subcircuits, we have

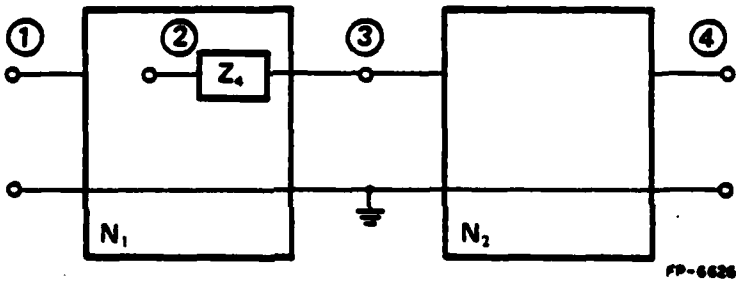


Fig. 4.7 An example of two circuits connected in tandem.

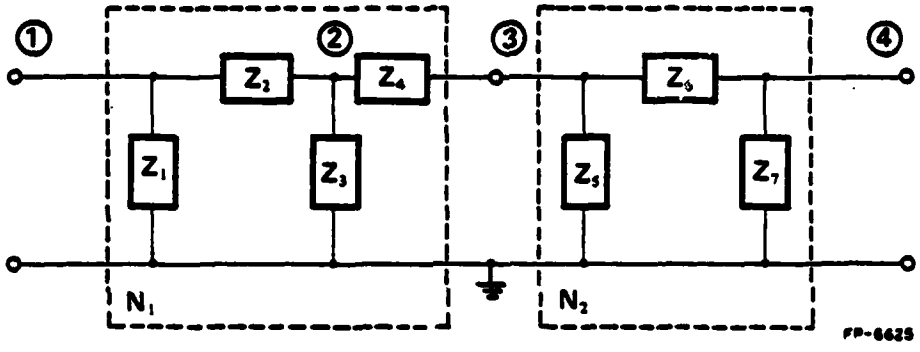


Fig. 4.8 An equivalent circuit for the circuit of the example.

accessibility to all the nodes which are the other end of all the elements connected to the output nodes of that subcircuit.

The same technique can be used for general situation, where we have more than two subcircuits connected in different ways.

CHAPTER 5

FAULT ANALYSIS IN ANALOG CIRCUITS WITH NONLINEAR ELEMENTS

In the previous chapters, the work was concentrated on linear circuits. However, we can extend the same approach to deal with circuits containing some nonlinear elements. This is simply because of the fact that Tellegen's power theorem is true also for nonlinear networks. In this case, we will see how to reformulate the equations in order to employ the idea of replacing each nonlinear element by its equivalent dc linear elements at that operating point. However, care should be taken when generating our linear equations using different measurement data. This is because the operating points of such nonlinear elements depend upon the measurement conditions. This difficulty may be overcome by the proper choice of adjoint circuits to isolate, first, the linear elements, then, the nonlinear elements, each at a time. This will yield the deviation in the linear elements, as well as one point on the characteristic of each nonlinear element.

As shown previously, assume we have a network N with b branches and m ports, where $\{V_k, I_k\}$ is the voltage across and current through the kth branch, respectively. Also, assume we have the adjoint circuit $\hat{N}$ with $\{\hat{V}_k, \hat{I}_k\}$ as the corresponding voltage and current of its kth branch, respectively. Assuming that both circuits obey Kirchhoff's laws, we can apply Tellegen's power theorem to get

$$0 = \sum_{k=1}^{b} (\hat{V}_k I_k - V_k \hat{I}_k) + \sum_{j=1}^{m} (\hat{V}_{pj} I_{pj} - V_{pj} \hat{I}_{pj}) \qquad \ldots.(5.1)$$

where V_{pj} and I_{pj} are the jth port voltage and current, respectively. Also, we apply the same theorem to the faulted circuit and the adjoint circuit to get

$$\sum_{k=1}^{b} [\hat{V}_k (I_k + \Delta I_k) - (V_k + \Delta V_k) \hat{I}_k] + \sum_{j=1}^{m} [\hat{V}_{pj} (I_{pj} + \Delta I_{pj}) - (V_{pj} + \Delta V_{pj}) \hat{I}_{pj}] = 0 \qquad \ldots.(5.2)$$

Rewrite Eq. (5.2) as

$$\sum_{k=1}^{b} \hat{V}_k (I_k + \Delta I_k) = \sum_{k=1}^{b} (V_k + \Delta V_k) \hat{I}_k - \sum_{j=1}^{m} [\hat{V}_{pj} (I_{pj} + \Delta I_{pj}) - (V_{pj} + \Delta V_{pj}) \hat{I}_{pj}] \qquad \ldots.(5.3)$$

By adding Eq. (5.1) to Eq. (5.3), we get

$$\sum_{k=1}^{b} \hat{V}_k (I_k + \Delta I_k) = \sum_{k=1}^{b} (\Delta V_k \hat{I}_k + \hat{V}_k I_k) + \sum_{j=1}^{m} (\Delta V_{pj} \hat{I}_{pj} - \hat{V}_{pj} \Delta I_{pj}) \qquad \ldots.(5.4)$$

For simplicity, assume that all the circuit elements are passive. Then, for linear elements we have

$$I_k = Y_k V_k \quad \text{,and} \quad I_k + \Delta I_k = (Y_k + \Delta Y_k)(V_k + \Delta V_k) \qquad \ldots.(5.5)$$

and for nonlinear elements, we have

$$I_k = f_k(V_k) \quad \text{,and} \quad I_k + \Delta I_k = F_k(V_k + \Delta V_k) \qquad \ldots.(5.6)$$

where f_k is the nominal nonlinear relation between current and voltage, and F_k is the corresponding faulty nonlinear relation, for the kth element. Then Eq. (5.4) will assume the form

$$\underline{h}^T \underline{x} = e \qquad \ldots.(5.7)$$

where

$$h_k = \begin{cases} \hat{V}_k & \text{;if the kth element is nonlinear} \\ \hat{V}_k(V_k + \Delta V_k) & \text{;if the kth element is linear} \end{cases} \qquad \ldots.(5.8)$$

and

$$x_i = \begin{cases} F_k(V_k + \Delta V_k) & \text{;if the kth element is nonlinear} \\ (Y_k + \Delta Y_k) & \text{;if the kth element is linear} \end{cases} \qquad \ldots.(5.9)$$

and

$$e = \sum_{k=1}^{b} (\Delta V_k \hat{I}_k + \hat{V}_k I_k) + \sum_{j=1}^{m} (\Delta V_{pj} \hat{I}_{pj} - \hat{V}_{pj} \Delta I_{pj}) \qquad \ldots(5.10)$$

Eq. (5.7) is linear in $\underline{x}$, although we have some nonlinear elements in the circuit N. By generating b equations of the form of Eq. (5.7), we can solve them to obtain the deviation in the linear elements and a point on the I-V characteristic of each nonlinear element. This system of linear equations could be obtained by associating different measurement data with different adjoint circuits. Since, for a nonlinear element, the corresponding unknown is its current, which depends nonlinearly upon its voltage, then the value of that unknown will vary under different test conditions. Hence, special choice of the adjoint circuits should be made in order to let the unknown,

corresponding to each nonlinear element, appear in only the equations generated under the same test condition. Appropriate short-circuits and equal voltage source excitations could be used to generate those different adjoint circuits. The following example will illustrate such techniques.

<u>Example</u>

Consider the ladder circuit shown in Figure 5.1, which has seven linear resistors and two nonlinear resistors. The different adjoint circuits are shown in Figure 5.2. The first adjoint circuit isolates R_1 and R_2. The second adjoint circuit isolates R_3 and R_4. The third adjoint circuit isolates R_5, R_6 and R_7. The fourth adjoint circuit isolates N.L.8, and the fifth adjoint circuit isolates N.L.9. For this example, three different test data are required. They may be obtained by exciting nodes 1,2 and 4 by a 1A current source, each at a time. By associating these adjoint circuits with three different test data, we get the following system of equations.

$$
\begin{array}{l}
\text{First adjoint circuit} \\
\text{+ two test data} \\
\text{Second adjoint circuit} \\
\text{+ two test data} \\
\text{Third adjoint circuit} \\
\text{+ three test data} \\
\\
\text{4th adj. ckt. +one t.d.} \\
\text{5th adj. ckt. +one t.d.}
\end{array}
\begin{bmatrix}
X & X & & & & & & & \\
X & X & & & & & & & \\
 & & X & X & & & & & \\
 & & X & X & & & & & \\
X & X & X & X & X & X & X & & \\
X & X & X & X & X & X & X & & \\
X & X & X & X & X & X & X & & \\
X & X & X & X & X & X & X & X & \\
X & X & X & X & X & X & X & & X
\end{bmatrix}
\begin{bmatrix}
G_1+\Delta G_1 \\
G_2+\Delta G_2 \\
G_3+\Delta G_3 \\
G_4+\Delta G_4 \\
G_5+\Delta G_5 \\
G_6+\Delta G_6 \\
G_7+\Delta G_7 \\
F_8(V_8+\Delta V_8) \\
F_9(V_9+\Delta V_9)
\end{bmatrix}
=
\begin{bmatrix}
X \\ X \\ X \\ X \\ X \\ X \\ X \\ X \\ X
\end{bmatrix}
\quad \ldots(5.11)
$$

where an X means a nonzero entry and a blank means a zero entry. Solving the first seven equations in Eq. (5.11), we get $(G_i+\Delta G_i)$, $i=1,2,\ldots,7$, while solving the last two equations, we get the current through N.L.8 and N.L.9 at the corresponding test conditions.

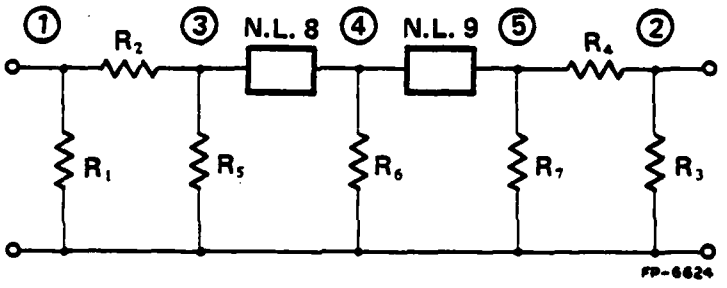


Fig. 5.1 An example of a circuit with two nonlinear elements.

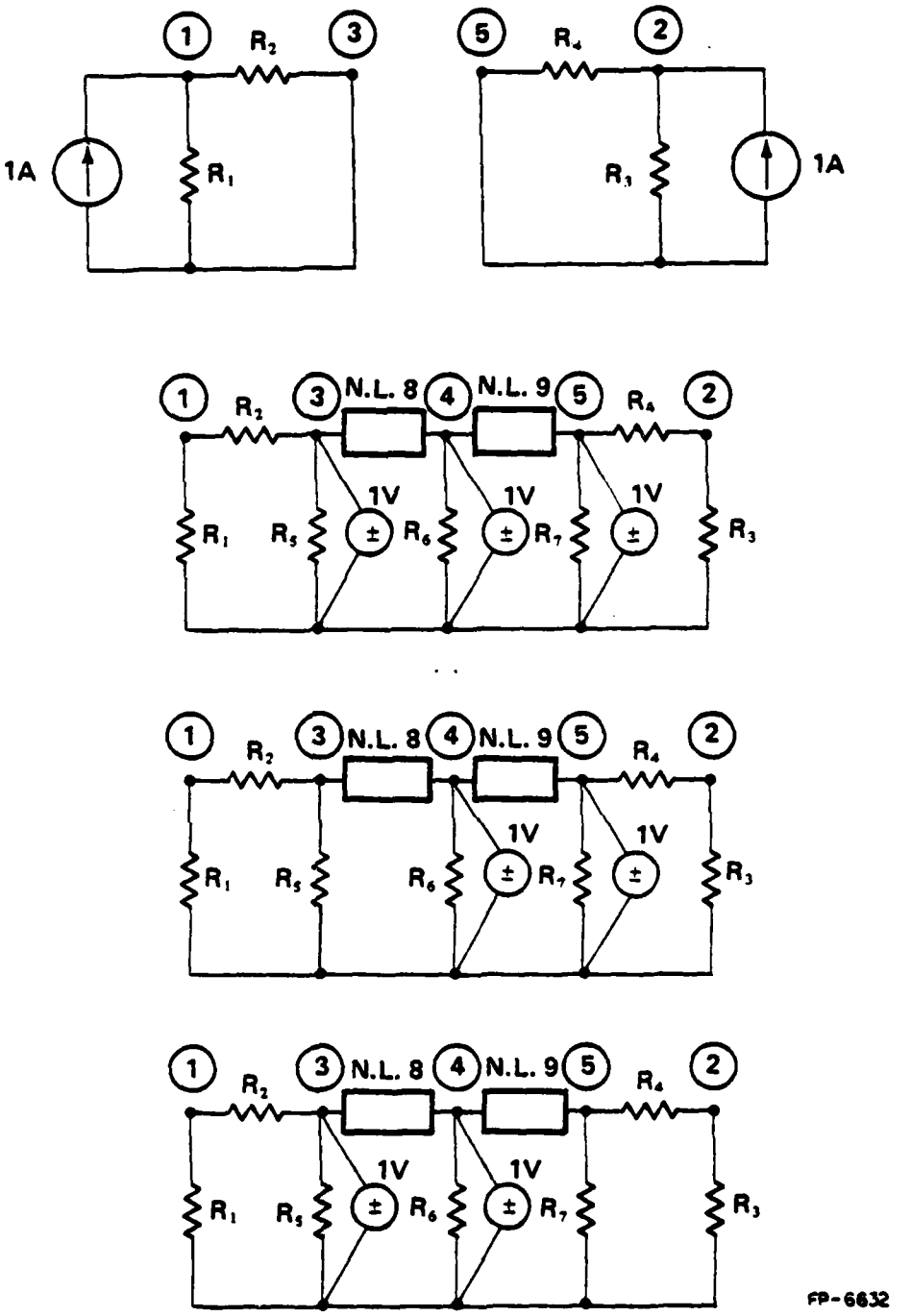


Fig. 5.2 The different adjoint circuits for the circuit of the example.

These currents will represent a point on the I-V characteristic of each nonlinear element. More points could be obtained by generating different equations under different test conditions.

It may be impossible to solve for some elements in some structures. Generally, the more nonlinear elements relative to the number of linear elements in a circuit , the more difficult it is to solve for the elements. Note that this technique may be applied in the dc test of a circuit with nonlinear elements, e.g.,diodes, transistors, etc. Then, after knowing the operating points for such elements, small signal models could be used for those elements in preparation for the ac small signal test.

CHAPTER 6

NUMERICAL EXAMPLES

In this chapter, some numerical examples are presented to demonstrate the application of the single fault detection algorithm in analog circuits. These examples were selected to cover almost every practical situation. They were solved on the DEC-10 computer system, which has a 36-bit word, using single precision arithmetic. In each example, the original circuit and the associated different adjoint circuits were simulated. Also, the faulty circuit was simulated under some different fault conditions as a substitute for the measurements.

Example 1:

Consider a 9th order Butterworth passive low pass filter [22] with a 3dB cutoff frequency of 1 rad/sec, as shown in Figure 6.1. Assume that only the input port (port 1) and the output port (port 2) are accessible. The nominal circuit parameter values, and the normalized sensitivities of I_{p1} and V_{p2} with respect to each parameter at $\omega = 0.5$ rad/sec are given below.

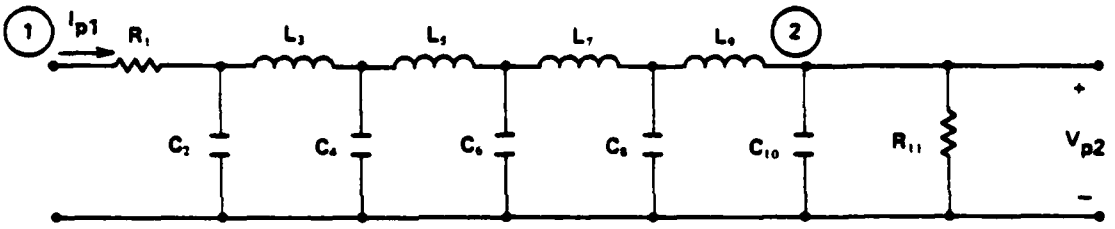


Fig. 6.1 9th order Butterworth passive low pass filter.

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
G_1	1.0000 Ω	0.5001752-j0.0010239	0.5001751-j0.0010239
C_2	0.3473 F	-0.0005329+j0.0867323	0.0001778-j0.0867946
F_3	1.0000 H	0.0873528+j0.2427349	0.0004661+j0.2578014
C_4	1.5320 F	0.3474672+j0.2239710	0.0003354-j0.4143348
Γ_5	1.8790 H	0.5085224-j0.1778165	-0.0005445+j.53792889
C_6	2.0000 F	0.0990011-j0.5785376	-0.0012198-j0.5871540
Γ_7	1.8790 H	-0.4168574-j0.3381497	-0.0005445+j0.5379289
C_8	1.5320 F	-0.4042586+j0.0937254	0.0003354-j0.4143348
Γ_9	1.0000 H	-0.1628680+j0.1993811	0.0004661+j0.2578014
C_{10}	0.3473 F	-0.0290323+j0.0817944	0.0001778-j0.0867946
G_{11}	1.0000 Ω	0.4710304+j0.1671885	-0.4998248-j0.0010239

A single fault is made in the element C_4 such that $\Delta C_4 = -0.332$ F (relative error = -0.21671), while the rest of elements assume their nominal values. The corresponding measurements (from the faulted circuit simulation) are given by

$$\frac{\Delta I_{p1}}{I_{p1}} = -0.0703694-j0.0548513$$

and, $$\frac{\Delta V_{p2}}{V_{p2}} = -0.0080688+j0.0890596$$

Then, the quantities $Diff_k = |C_k^{(1)}-C_k^{(2)}|$; k=1,2,.....,11 , are calculated and found to be

Element	$Diff_k$
R_1	0.3135244E+00
C_2	0.9899682E+00
L_3	0.6558627E+00
C_4	0.9680828E-07
L_5	0.2981575E+00
C_6	0.2536567E+00
L_7	0.1807123E-01
C_8	0.3967876E+00
L_9	0.4613443E+00
C_{10}	0.1276600E+01
R_{11}	0.2216817E+00

Because of the limited accuracy of a computer, it is expected that the difference corresponding to the faulty element will not be zero. However, it will be very small compared to the differences corresponding

to the other nonFaulty elements. Accordingly, from the above values, it is clear that the faulty element is C_4. The value of α_4 is calculated using Eq. (18) of the fourth chapter and found to be -0.0003354+j0.4143348. Then Eq. (4.14) of the fourth chapter is used to calculate the value of the relative error in C_4, which is found to be -0.2167102+j0.0 .This calculated relative error value agrees with the exact value .

Another single fault is made in the element R_{11} such that ΔG_{11} = -0.285714 Ω^{-1} (relative error = -0.285714), while the rest of elements assume their nominal values. The following is the corresponding values of $Diff_k$ for each element.

Element	$Diff_k$
R_1	0.6566101E+00
C_2	0.6401004E+00
L_3	0.1217485E+01
C_4	0.4993380E+00
L_5	0.2676563E+00
C_6	0.5655879E+00
L_7	0.3575838E+00
C_8	0.3863488E+00
L_9	0.1273844E+01
C_{10}	0.3914174E-06
R_{11}	0.6386881E-07

From the above values, C_{10} and R_{11} appear to be faulty. This is because they are in parallel. The value of α_{10} is -0.0001778+j0.0867946 and the value of α_{11} is 0.4998248+j0.0010239. The calculated relative error in C_{10} is 0.0+j1.6453459, while the calculated relative error in G_{11} is -0.2857143+j0.0 . This shows that G_{11} is the true faulty element because the relative error value must be real. The calculated value of the relative error in G_{11} agrees with the exact value .

Example 2:

Consider the simple transistor amplifier circuit [6] shown in Figure 6.2. Assume that we have access only to the input port (port 1) and the output port (port 2). The nominal circuit parameter values and the sensitivities of I_{p1} and V_{p2} with respect to each circuit parameter at ω= 502 rad/sec are given below (this frequency is chosen to be in the neighborhood of a low frequency pole).

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
C_1	0.478 μF	0.2298527-j0.4090646	0.2298527-j0.4090645
$G_{2,3}$	8.420 kΩ	0.7171331+j0.3594040	-0.2024641+j0.3811799
G_4	5.100 kΩ	-0.0033117-j0.0005916	-0.5814817+j0.1780174
G_5	1.000 kΩ	0.0591370+j0.0262817	0.8450619-j0.2744815
C_6	0.683 μF	-0.0090111+j0.0202761	0.0941104+j0.2897430
C_7	0.446 μF	-0.0016268-j0.0000381	0.1588052-j0.3660625
G_8	5.210 kΩ	0.0000444-j0.0018976	-0.5729964+j0.1852427
G_{ie}	3.610 kΩ	0.0524703+j0.0491858	-0.0373001+j0.0280279
h_{re}	0.000290	0.0000624+j0.0000599	0.0011573+j0.0000472
gm	0.0288	-0.0510448-j0.0467522	0.0731976-j0.0162581
h_{oe}	35.75 kΩ	0.0063583+j0.0031935	-0.0067837+j0.0036589
C_{oe}	26.00 pF	-0.0000015+j0.0000030	-0.0000017-j0.0000032

where $G_{2,3}$ is the parallel combination of G_2 and G_3.

A single fault is made in the element C_7 such that ΔC_7 = 0.054 μF (relative error = 0.1210762), while the rest of the elements assume their nominal values. The faulted circuit is simulated and the measurements are obtained. Then, the $Diff_k$ corresponding to each element is calculated. These differences are given below.

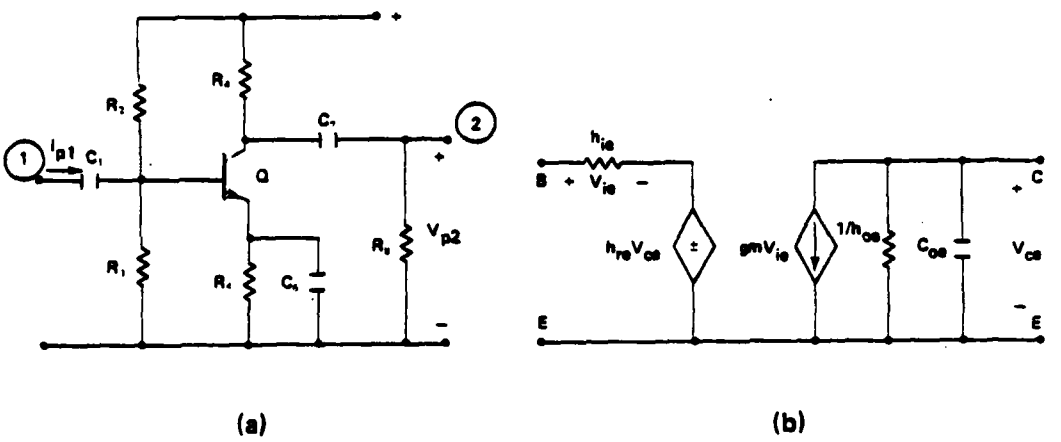


Fig. 6.2 (a) Simple transistor amplifier circuit.
(b) Small signal model for the transistor.

Element	$Diff_k$
C_1	0.9351468E-01
$R_{2,3}$	0.1012977E+00
R_4	0.1175077E+00
R_5	0.5180476E-01
C_6	0.1510933E+00
C_7	0.6867184E-05
R_8	0.1563013E+00
h_{ie}	0.9365815E+00
h_{re}	0.3968770E+02
gm	0.5817796E+00
h_{oe}	0.5659735E+01
C_{oe}	0.1214649E+05

This shows that C_7 is the faulty element. Then α_7 is calculated to 0.8411948+j0.3660625 , and the relative error is 0.1210727+j.0000025 , which agrees with the exact value to some accuracy.

Another single fault is made in C_6 such that ΔC_6 = -0.68232 μF (relative error = -0.999), while the rest of the circuit elements assume their nominal values. In this case, the differences corresponding to each element are given below.

Element	$Diff_k$
C_1	0.6211047E+00
$R_{2,3}$	0.7323908E+00
R_4	0.6174266E+01
R_5	0.3114448E-06
C_6	0.9059803E-06
C_7	0.1447078E+02
R_8	0.1162000E+02
h_{ie}	0.6843163E+01
h_{re}	0.6830308E+01
gm	0.4419909E+01
h_{oe}	0.4299827E+02
C_{oe}	0.9227960E+05

This shows that both R_5 and C_6 are faulty, although only C_6 is the true faulty element. This is expected because R_5 and C_6 are in parallel. However, when we calculate the relative error in R_5, we get

3167.96-j3096.43 , while for C_6 we get -0.9990002-j0.0000004. It is clear from these values that C_6 is the true faulty element, because the relative error must be real.

A third single fault is made in h_{oe} such the $\Delta h_{oe} = 0.02798\ \Omega^{-1}$ (relative error = 999.0), while the rest of circuit parameters assume their nominal values. The differences corresponding to each element are given below.

Element	$Diff_k$
C_1	0.3357031E+01
$R_{2,3}$	0.1385590E+01
R_4	0.2546923E+03
R_5	0.1418424E+02
C_6	0.4136963E+02
C_7	0.5215209E+03
R_8	0.4499215E+03
h_{ie}	0.1035142E+02
h_{re}	0.1063342E+05
gm	0.9078709E-06
h_{oe}	0.8753567E-05
C_{oe}	0.1792730E-01

Again, since gm and h_{oe} are in parallel, they both appear faulty. However, when we calculate the relative error in both gm and h_{oe}, we get -0.1135017-j0.0615357 for gm and 999.000-j0.0000357 for h_{oe}. This indicates that h_{oe} is the true faulty element, because the relative error must be real.

Example 3:

Consider the Sallen and Key low pass filter [23] shown in Figure 6.3. The circuit parameter nominal values, and the sensitivities of I_{p1} and V_{p2} with respect to the circuit parameters are given below (ω = 1.0E5 rad/sec).

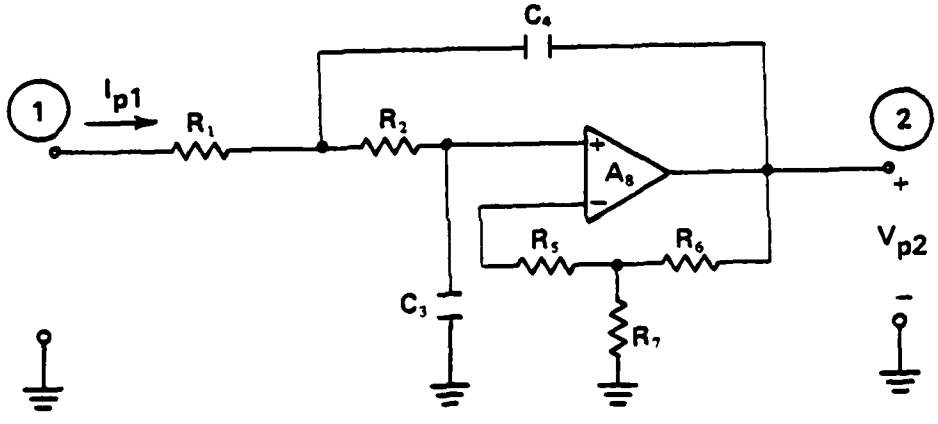


Fig. 6.3 Sallen and Key low pass filter.

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
G_1	50.00 kΩ	0.6098415+j0.6212523	0.6098415+j0.6212522
G_2	100.0 kΩ	0.0862345+j0.1465388	1.0713967+j0.2674421
C_3	1.070 nF	-0.3109863-j0.3293604	-1.3442544-j0.0582801
C_4	1.000 nF	0.6149102-j0.4384307	-0.3369839-j0.8304142
G_5	128.7 kΩ	0.0000000+j0.0000000	0.0000000+j0.0000000
G_6	50.00 kΩ	0.1554304+j0.1264330	0.6139787-j0.1446491
G_7	37.00 kΩ	0.1554304+j0.1264330	0.6139787-j0.1446491
A_8	100000.	0.0000064+j0.0000052	0.0000251-j0.0000059

The following describes some different single faults together with their obtained results.

(a) Single fault in G_1 (exact relative error = 0.020408)

$Diff_1$ = 0.2387080E-07

α_1 = 0.3901585-j0.6212522

Calculated relative error = 0.0204082+j0.0

(b) Single fault in G_2 (exact relative error = 999.0)

$Diff_2$ = 0.2002193E-04

α_2 = -0.0713968-j0.2674421

Calculated relative error = 1000.60+j0.3716239

(c) Single fault in C_3 (exact relative error = 99.0)

$Diff_3$ = 0.1575698E-07

α_3 = 1.3442544+j0.0582801

Calculated relative error = 99.0054-j0.0000995

(d) Single fault in C_4 (exact relative error = 9.0)

$Diff_4$ = 0.5215406E-07

α_4 = 0.3369839+j0.8304143

Calculated relative error = 9.0000011+j0.0000017

(e) Single fault in G_6 (exact relative error = 9.0)

$Diff_6$ = 0.1493024E-07

$Diff_7$ = 0.2252569E-07

α_6 = 1.1886913-j0.1446491

α_7 = 0.1886913+j0.1446491

Calculated relative error in G_6 = 8.9999937+j0.00000535

Calculated relative error in G_7 =-9.0000000-j0.00000010

It is clear that both G_6 and G_7 appear faulty. This is because $S_{G_6}^{I_{p1}} = S_{G_7}^{I_{p1}}$ and $S_{G_6}^{V_{p2}} = S_{G_7}^{V_{p2}}$. However, from the calculated relative error value for G_7, we can see that if R_7 is the true faulty element, then $R_7+\Delta R_7$ must be a negative resistance, which is not possible for this example. Then R_6 is the true faulty element.

Example 4:

Consider a Friend circuit realizing a 2nd order high pass notch filter [24], Figure 6.4. The circuit parameter nominal values and the sensitivities of I_{p1} and V_{p2} with respect to the circuit parameters are given below (ω= 3500 rad/sec).

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
G_1	13.20 kΩ	-0.0002954+j0.7814375	-2.0971564+j8.9101788
G_2	93.00 kΩ	-0.6904411-j0.0429325	-8.4262893-j1.6020173
G_3	214.0 kΩ	0.1998532+j0.0450179	2.2899989+j0.8563859
G_4	2.000 kΩ	0.1866924-j0.7257722	-2.2215950-j8.9730738
G_5	2.000 kΩ	0.4291944+j0.5167088	1.0913519+j6.3913345
G_6	12.47 kΩ	-0.2432444-j0.4178438	-2.7126559-j5.1676651
G_7	10.00 kΩ	0.2352070+j0.1729853	1.1302431+j2.5817394
C_8	0.010 nF	0.4631123-j0.1010907	5.7611653-j0.4630128
C_9	0.010 nF	0.4199217-j0.2285105	5.1849374-j2.5338697
A_{10}	10000.	0.0000971+j0.0001058	0.0010032+j0.0014338

The following describes some different single faults and their obtained results.

(a) Single fault in G_1 (exact relative error = 0.32)

$Diff_1$ = 0.1945216E-07

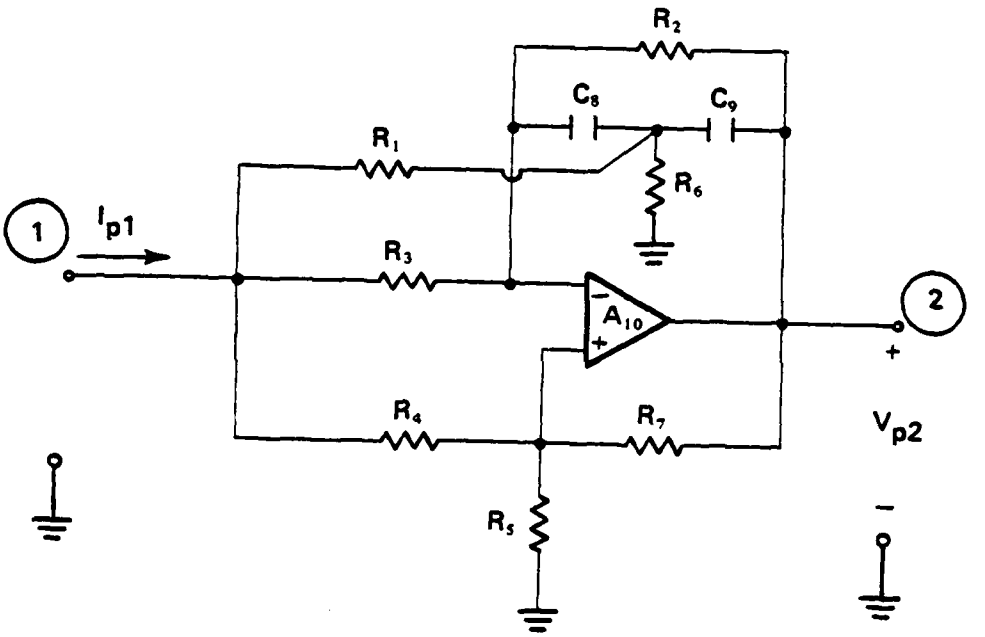


Fig. 6.4 2nd order high pass notch filter (Friend circuit).

α_1 = 1.4291995-j1.3568168

Calculated relative error = 0.3199999+j0.0

(b) Single fault in G_2 (exact relative error = 9999.0)

$Diff_2$ = 0.1490755E-07

α_2 = 4.4014133-j0.0438022

Calculated relative error = 10008.691+j2.333323

(c) Single fault in G_3 (exact relative error = 0.019048)

$Diff_3$ = 0.1758195E-07

α_3 =-0.1910450+j0.0019013

Calculated relative error = 0.0190477+j0.0

(d) Single fault in G_4 (exact relative error = 0.0050251)

$Diff_4$ = 0.2348175E-07

α_4 = 0.8690785+j0.5924875

Calculated relative error = 0.0050252

(e) Single fault in C_8 (exact relative error = -0.1)

$Diff_8$ = 0.2734057E-07

α_8 =-2.8495944+j0.8248030

Calculated relative error = -0.1+j0.0

Example 5:

Consider a Friend circuit realizing a 2nd order band pass filter with center frequency of 1.0 kHz and a bandwidth of 100.0 Hz, Figure 6.5. The circuit parameter nominal values and the sensitivities of I_{p1} and V_{p2} with respect to the circuit parameters are listed below (ω= 7000 rad/sec).

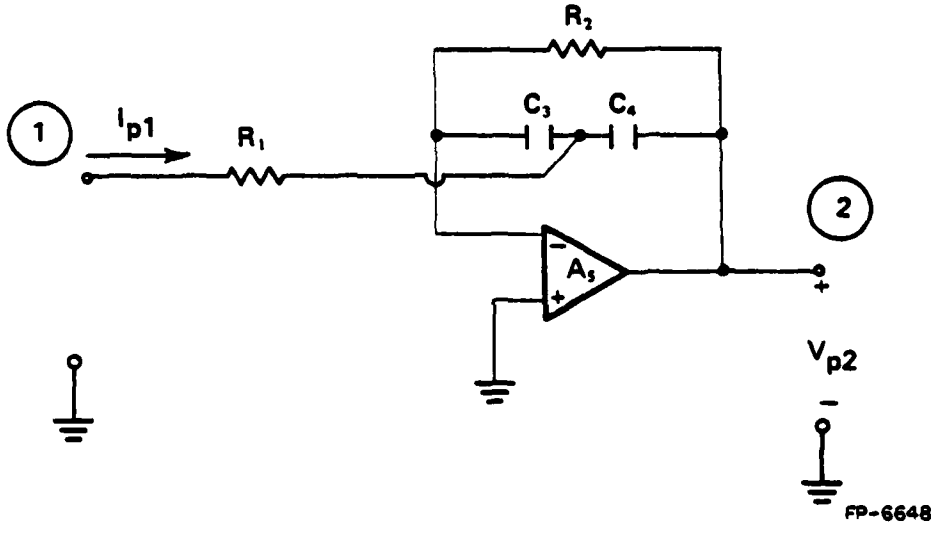


Fig. 6.5 2nd order band pass filter (Friend circuit).

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
G_1	1.000 k Ω	4.4141764+j1.5810643	4.4141763+j1.5810642
G_2	400.0 k Ω	3.2464605+j1.8716715	3.2384681+j1.9607132
C_3	7.958 nF	-3.3304946-j1.7259875	-3.3264983-j1.7705083
C_4	7.958 nF	-3.3301424-j1.7267483	-4.3261462-j1.7712691
A_5	10000.	0.0003521-j0.0007608	0.0003621-j0.0007608

The following describes some different single faults and their obtained results.

(a) Single fault in G_1 (exact relative error = 9.0)

$Diff_1$ = 0.5665014E-08

α_1 =-3.4141764-j1.5810642

Calculated relative error = 8.9999945+j0.0000069

(b) Single fault in G_2 (exact relative error = 0.14286)

$Diff_2$ = 0.2634178E-08

α_2 =-3.2384681-j1.9607133

Calculated relative error = 0.1428571+j0.0

(c) Single fault in C_3 (exact relative error = 9.0)

$Diff_3$ = 0.8330002E-08

α_3 = 4.3264983+j1.7705083

Calculated relative error = 8.999995+j0.0000010

(d) Single fault in C_4 (exact relative error = -0.12027)

$Diff_4$ = 0.2082501E-08

α_4 =-4.3261462+j1.7712691

Calculated relative error = -0.1203599+j0.0

Example 6:

Consider a 4th order Butterworth low pass filter using the FDNR concept [25], Figure 6.6, with 3dB cutoff frequency of 1.0 kHz. The circuit parameter nominal values, and the sensitivities of I_{p1} and V_{p2}

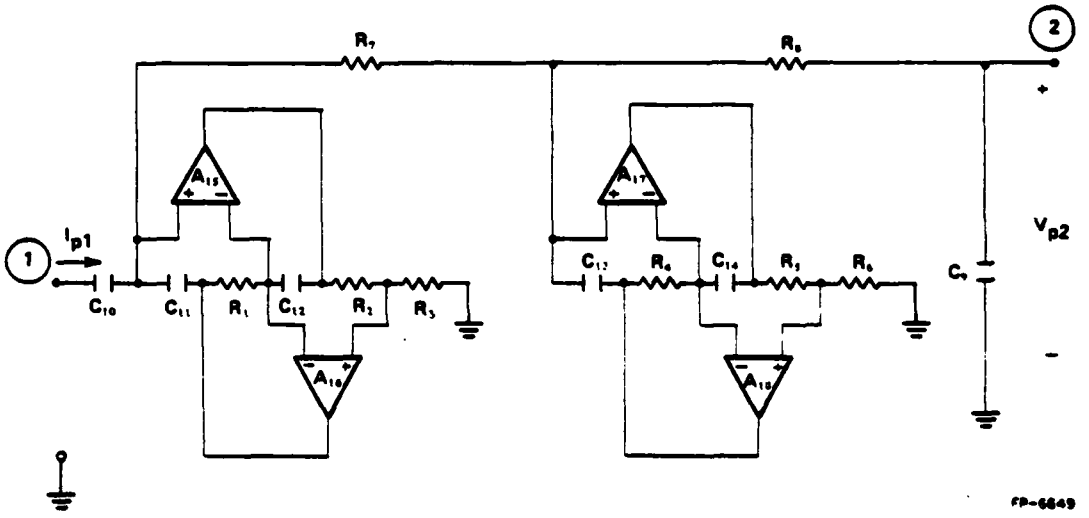


Fig. 6.6 4th order Butterworth low pass filter using the FDNR concept.

with respect to the circuit parameters are listed below (ω = 7000 rad/sec).

Parameter(P_i)	Nominal Values	$S_{P_i}^{I_{p1}}$	$S_{P_i}^{V_{p2}}$
G_1	1.000 kΩ	-3.4247676-j0.9295328	0.1358290+j0.7569033
G_2	1.000 kΩ	-3.4235955-j0.9295252	0.1357217+j0.7566731
G_3	1.000 kΩ	3.4235955+j0.9295252	-0.1357217-j0.7566731
G_4	1.000 kΩ	-0.4165778-j1.2889606	1.2634121+j1.0013481
G_5	1.000 kΩ	-0.4169069-j1.2885058	1.2634377+j1.0006804
G_6	1.000 kΩ	0.4169069+j1.2885057	-1.2634376-j1.0006804
G_7	29.30 kΩ	-3.2199468-j1.9502319	1.2667378+j1.0014152
G_8	12.10 kΩ	0.3211149-j0.0476300	01.311967+j0.7523334
C_9	0.010 μF	-0.0562338-j0.3791203	-0.1117670-j0.1548958
C_{10}	0.010 μF	0.1136902+j0.1588125	0.1133559+j0.1588170
C_{11}	34.93 nF	3.4254839+j0.9268999	-0.1364110-j0.7567992
C_{12}	34.93 nF	3.4239223+j0.9310275	-0.1354578-j0.7568765
C_{13}	54.22 nF	3.4239223+j0.9310275	-0.1354578-j0.7568765
C_{14}	54.22 nF	0.1466997+j1.2888574	-1.2634646-j1.0011655
A_{15}	10000.	-0.0000768+j0.0029860	0.0005918-j0.0002621
A_{16}	10000.	-0.0007301-j0.0000184	0.0000641+j0.0001447
A_{17}	10000.	-0.0005957+j0.0004772	0.0002748-j0.0008658
A_{18}	10000.	-0.0001812-j0.0002260	0.0003286+j0.0001042

The following describes some different single faults with their obtained results.

(a) Single fault in G_7 (exact relative error = 0.95333)

$Diff_7$ = 0.1002608E-03

α_7 =-0.2670898-j1.0012017

Calculated relative error = 0.953617-j0.000120

(b) Single fault in C_9 (exact relative error = 1.0)

$Diff_9$ = 0.1101016E-02

α_9 = 0.111767+j0.1548958

Calculated relative error = 1.0001145+j0.0001555

(c) Single fault in C_{10} (exact relative error = -0.3)

$Diff_{10}$ = 0.5822352E-02

α_{10} = 0.8863097-j0.1588125

Calculated relative error = -0.3009755-j0.0007091

(d) Single fault in G_8 (exact relative error = -0.19333)

$Diff_8$ = 0.9969877E-04

α_8 = 0.8688033-j0.7523333

Calculated relative error = -0.19333842+j.0000181

From these examples, we find that in some circuits, e.g., circuits containing op-amps, we may not be able to detect single faults due to some equal sensitivity values. The same situation happens when we have two or more parallel elements. However, in this case if they are different types, they can be separated.

CHAPTER 7

CONCLUSION

A method has been presented for the calculation of large circuit component variations, based on the adjoint circuit concept. The method requires that the node voltages of the circuit be available. In this case, there exists a linear relationship between large parameter deviations and the test port measurements in a linear circuit. Given these measurements, the values of the components can be easily computed by solving a set of linear algebraic equations. Furthermore, the formulation of the method allows one to determine necessary and sufficient test conditions required to determine the component values. The accuracy of the method in the presence of measurement errors depends upon the structure of the circuit and its component values.

In the absence of sufficient test measurements due to the inaccessibilty of some nodes in a circuit, the method could be used to isolate the faulty components to some subset of the components in the circuit. It has been shown that simple input and output port voltage measurements are enough to determine a single fault. The same approach is implemented at the block level, where the faulty blocks in a circuit can be identified.

The same approach could be used to identify faults in circuits with some nonlinear components. Special choice of the adjoint circuits enables one to isolate the linear elements from the nonlinear elements

allowing one to obtain a different bias point on the I-V characteristic of every nonlinear element.

These results were used for the fault analysis of some analog circuit examples, and the results show excellent agreement with the theory.

More investigation is needed for the detection of multiple faults given a limited number of accessible nodes, especially when some of the nonfaulty elements are within a specified tolerance of their nominal values. Also, necessary and sufficient conditions need to be determined in order to locate these multiple faults, rather than to isolate them in a subgroup of the circuit elements. Furthermore, the application of the single fault algorithm on active circuits with nonzero-toleranced parameters needs to be applied to some examples in order to compare the algorithm computationally with the fault dictionary approach. Finally, a comprehensive computer program needs to be written for the single and multiple fault detection and isolation that takes care of all the practical situations that exist in practice.

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